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Enhanced stability of Ni monosilicide on MOSFETs poly-Si gate stack

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Abstract

The formation and stability of Ni(Pt)Si on metal oxide semiconductor field effect transistor (MOSFETs) polycrystalline-Si (poly-Si) gate stack was investigated. Poly-Si and partial amorphous Si (a-Si) structures were grown using LPCVD and RTCVD techniques. For pure Ni silicidation, nucleation of $NiSi_2$ was found at 700°C, which is slightly lower than that on monocrystalline Si (about 750°C). With Pt addition, Ni(Pt)Si was found up to 800°C, implying the important role of Gibbs free energy changes in enhancing the monosilicide stability. The extent of layer inversion of Ni(Pt)Si on RTCVD-Si is less than that on LPCVD-Si and thus results in a slower sheet resistance degradation. © 2002 Elsevier Science B.V. All rights reserved.

Keywords: Ni(Pt)Si; Ni silicidation; RTCVD; LPCVD; Layer inversion

1. Introduction

SALICIDE (self-aligned silicide) technology has become an essential part of the fabrication process for recent high speed CMOS logic circuits. Silicides allow a reduction in the parasitic resistance of integrated circuits, especially, in the sheet and contact resistance of the polysilicon gate and the diffused single crystal silicon (or active regions), which are major causes of performance degradation in deep submicron CMOS devices. $TiSi_2$ has been used almost exclusively as a salicide material for submicron devices before the introduction of $CoSi_2$ for sub 0.25 μm devices. The need to replace

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$TiSi_2$ is due to the increased sheet resistance of narrow lines caused by incomplete transformation from the C49 to C54 phase. In view of the high Si consumption and junction leakage problem in $CoSi_2$, investigation of NiSi as a replacement material for salicidation has received considerable attention. The formation by one step low temperature annealing, the low Si consumption during NiSi formation, and the absence of the linewidth dependence of the sheet resistance are among the advantages of NiSi.

NiSi can be formed at temperature as low as 300°C with diffusion controlled reaction. The phase transformation from NiSi to $NiSi_2$ is known to be a nucleation-controlled process and occurs at temperatures of 750°C and above [1]. The $NiSi_2$ formation is undesirable for ultra shallow junction applications since $NiSi_2$ has a high resistivity and consumes more Si during its formation. The stability of silicide at high temperature is also crucial for applications in new merged devices, such as logic and DRAM, logic and RF, DRAM and RF, in which various thermal processes will be needed. Therefore, much effort has been channeled to retard the $NiSi_2$ nucleation to a higher temperature to allow a higher backend processing temperature and a wider salicidation processing window.

Besides the undesirable phase transformation at elevated temperatures, thermal degradation of the silicide film is of much concern. Agglomeration of NiSi films has been reported at annealing temperatures as low as 600°C [2]. Silicide/polycrystalline Si (polycide) structure is more vulnerable to thermal degradation than silicide/monocrystalline Si. On undoped polycrystalline Si (poly-Si), layer inversion that corresponds to the inversion in the respective position of the silicide and the poly-Si was reported to start at 550°C [3]. The driving force for layer inversion to occur has been attributed to poly-Si grain growth in order to reduce the grain boundary energies. The use of Ni(Pt) alloy has been shown to enhance the stability of the monosilicide (Ni(Pt)Si) on Si(100) and Si(111) up to 900°C by retarding the formation of the high resistivity $NiSi_2$ phase [4]. It is of interest to study the effect of Pt on Ni silicidation on poly-Si, which is of considerable importance for various applications.

2. Experimental procedures

p-Type Si(100) wafers were used in this study. Polycrystalline Si (poly-Si) of thickness 250 nm was grown using the conventional low pressure chemical vapor deposition (LPCVD) on top of 60 Å gate oxide to form a gate stack for MOSFETs applications. The LPCVD poly-Si growth was done at 620°C, 0.2 Torr, which resulted in needle-like columnar poly-Si grains. To compare the effect of Si microstructures on the silicide formation and stability, rapid thermal chemical vapor deposition (RTCVD) was used to grow a different gate stack. RTCVD process was carried out in a single wafer in-situ processing multichamber cluster tool, which allows the subsequent growth of gate oxide and poly-Si without breaking vacuum and with high throughput. The gate stack comprises of a 24 Å gate oxide and a 2000 Å Si film which was grown at 680°C for 130 s with a deposition pressure of 60 Torr. RTCVD deposition process is initiated and terminated by rapid changes in the substrate temperature, providing precise control of the process time down to a few seconds. Therefore, the films can be deposited at higher temperatures for short time resulting in low thermal budgets. The two kinds of gate stacks were sputtered with Ni(Pt) of about 26 nm and subjected to rapid thermal annealing at temperatures ranging from 500 to 900°C in N_2 ambient for 1 min. The amount of Pt is about 5 at.%. The silicided films were analyzed using cross section transmission electron microscopy (XTEM),

X-ray diffraction (XRD), Rutherford backscattering spectrometry (RBS), micro-Raman spectroscopy and sheet resistance measurements.

3. Results

Fig. 1 shows an XTEM image of the as-deposited Ni(Pt) film on the as-grown RTCVD poly-Si. As observed from the micrograph and diffraction analysis, the upper half of the Si layer is amorphous whereas the lower half of the film consists of randomly oriented Si grains with irregular sizes and shapes. The amorphous and polycrystalline interface is not well defined and nonuniform. For Si nucleation on SiO_2 in RTCVD growth, large and sparse disk-like nuclei were observed for growth temperatures greater than 660°C [5]; the RTCVD growth mechanism in the present study should be similar. The low nuclei density and a rough crystalline/amorphous interface obtained is possibly a result of a high processing temperature which leads to high deposition rate. As-deposited LPCVD poly-Si films have columnar grains as reported previously and is the result of growth from a high density of critical nuclei at a given pressure and temperature [6]. Further heat treatment does not affect the grain growth significantly until above 1100°C [6,7]. Above this temperature, grain growth

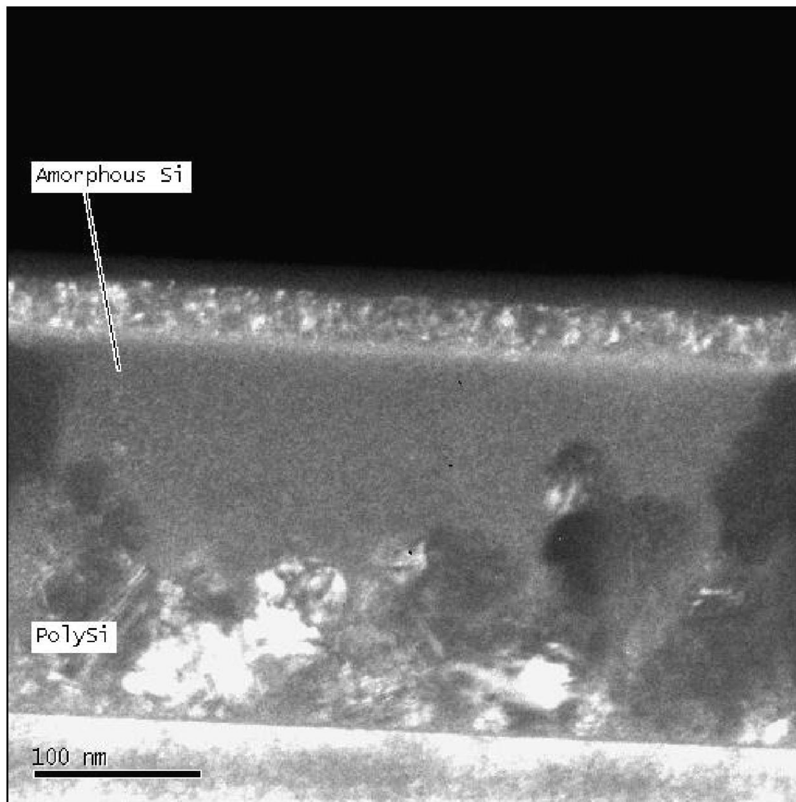

Fig. 1. XTEM (dark field) image of as-deposited Ni(Pt) film on RTCVD-Si.

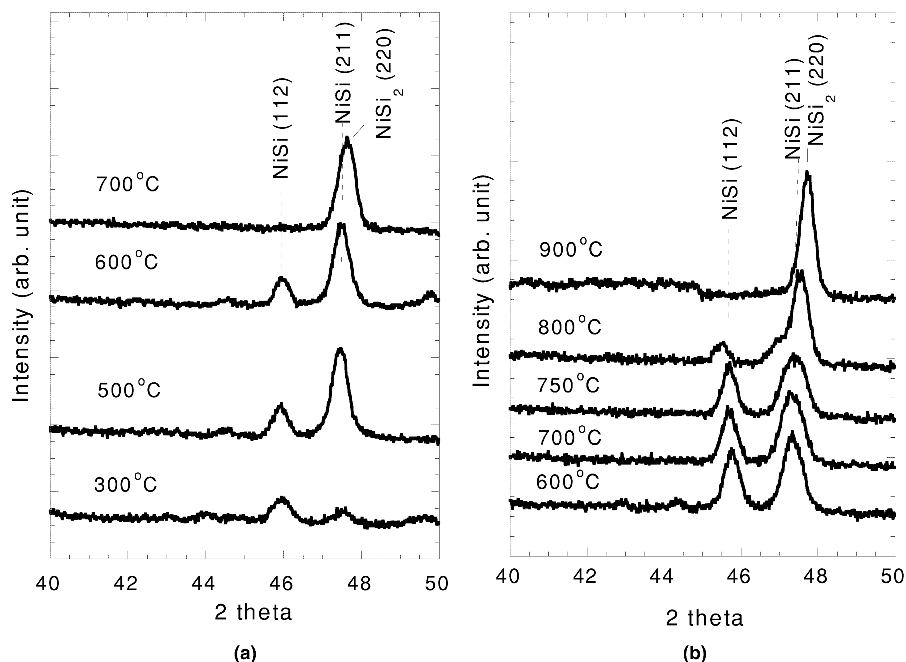

Fig. 2. (a) Grazing incidence XRD analysis of Ni on RTCVD-Si and (b) Ni(Pt) on RTCVD-Si after annealing at various temperatures.

occurs by the nucleation and growth of fault-free new crystals at the expense of the faulted deposited grains [6].

Fig. 2(a) and (b) shows the grazing incidence XRD analysis of the Ni and Ni(Pt) films on RTCVD-Si after annealing at various temperatures. Pure Ni and Ni(Pt) silicidation leads to the formation of monosilicide at 500°C as indicated by the XRD peaks corresponding to (112) NiSi and (211) NiSi. It was observed that NiSi is absent at 700°C anneal for pure Ni but exists up to 800°C for Ni(Pt) silicidation. From this temperature onwards, peaks corresponding to $NiSi_2$ are present (peak (220) $NiSi_2$ in Fig. 2). The peaks corresponding to $NiSi_2$ might be overlapping with those of polycrystalline Si because of the closely related structures of $NiSi_2$ and Si but the peak positions give lattice spacing closer to that of $NiSi_2$. The XRD spectra for Ni and Ni(Pt) silicide films formed on the LPCVD poly-Si substrates are shown in Fig. 3(a) and (b) and are similar to that on RTCVD-Si. NiSi is still present after annealing at temperatures up to 800°C for Ni(Pt). For pure Ni, NiSi is present only below 700°C. At higher annealing temperature, the nucleation of $NiSi_2$ has taken place. The addition of Pt has thus led to the stabilization of the NiSi phase up to a temperature of 750–800°C for both polycide structures. In contrast, NiSi was not detected for pure Ni on LPCVD poly-Si and RTCVD-Si after annealing at 700°C and above and thus $NiSi_2$ seems to nucleate at lower temperature on poly-Si compared to that on monocrystalline Si where the nucleation usually occurs at 750°C.

The XRD results are further confirmed using Raman spectroscopy as shown in Fig. 4. Ni(Pt)Si Raman peaks at wavenumber 213 cm^{-1} [8] can be observed after annealing at temperatures up to 800°C on RTCVD-Si and LPCVD poly-Si. However, no NiSi Raman peaks can be detected from

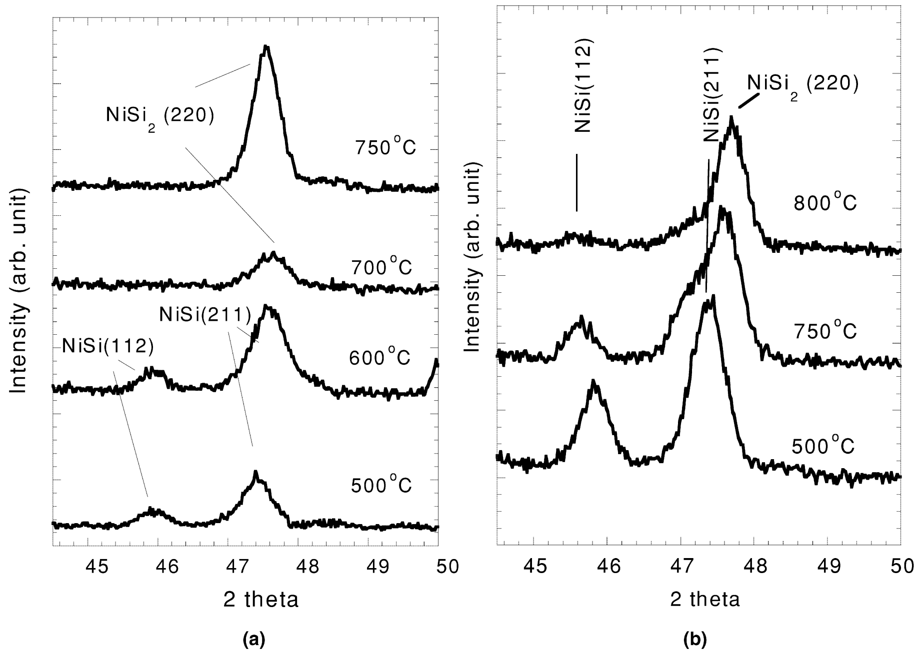

Fig. 3. (a) Grazing incidence XRD analysis of Ni on LPCVD poly-Si and (b) Ni(Pt) on LPCVD poly-Si after annealing at various temperatures.

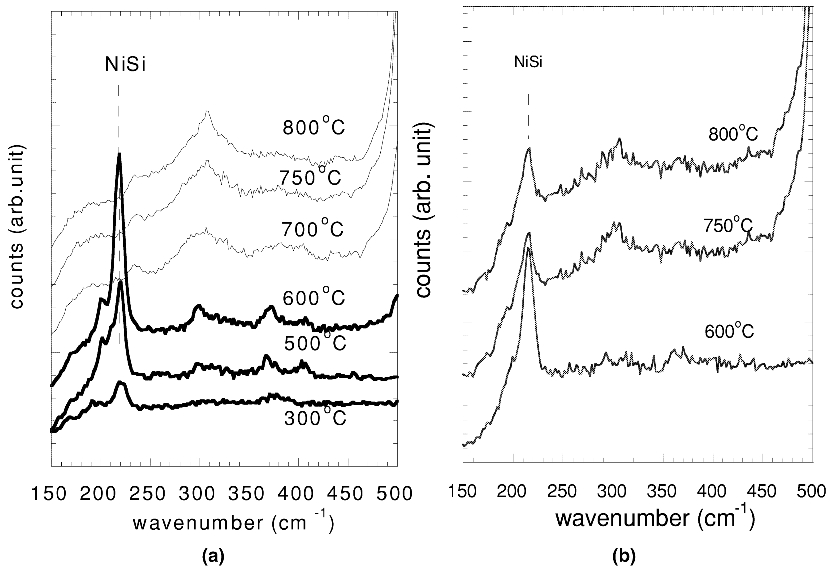

Fig. 4. (a) Raman spectra of Ni on RTCVD-Si and (b) Ni(Pt) on RTCVD-Si after annealing at various temperatures.

700°C onwards for pure Ni on RTCVD and LPCVD-Si in agreement with the XRD measurements. This confirms that NiSi is absent at 700°C on both types of gate stack with pure Ni silicidation.

The sheet resistance measurement provides a sensible technique to understand the extent of morphology degradation that includes poly-Si inversion and agglomeration of silicides. Fig. 5 shows the sheet resistance measurement of the Ni(Pt) silicides formed at various temperatures for Ni(Pt) on RTCVD-Si and LPCVD poly-Si. On LPCVD poly-Si, the sheet resistance increased dramatically at temperatures as low as 600°C. The rapid increase in sheet resistance as a function of silicidation temperatures is likely due to the occurrence of layer inversion. It can be observed that the sheet resistance degradation is less severe for silicides formed on the RTCVD-Si particularly at the temperatures of 600 and 700°C, at which the sheet resistance is an order of magnitude lower than that of the LPCVD poly-Si. This indicates that morphology degradation is less extensive on the RTCVD-Si substrates.

The sheet resistance data can be correlated with the respective RBS spectra. Fig. 6 shows the RBS analysis of the Ni silicide films formed by annealing of Ni(Pt)/LPCVD-Si and Ni(Pt)/RTCVD-Si samples at various temperatures. It was found that at 500°C, a uniform layer of Ni(Pt)Si with Pt of about 5 at.% was formed on LPCVD poly-Si. For silicide formation at 600°C (Fig. 6a), the RBS spectrum displays a broadening and lowering of the Ni and Pt signal. The relative yield shows high silicon concentration at the surface. This corresponds to layer inversion, i.e. the reversal of the silicide and poly-Si layer position has occurred at temperatures as low as 600°C. Similar results were obtained for the study of pure Ni on poly-Si [3]. At silicidation temperature of 700°C, the inverted layer becomes more homogeneous with the average silicon concentration exceeding 90% at the surface.

On the RTCVD-Si substrates, the RBS spectrum at 600°C (Fig. 6b) shows a layer of Ni(Pt)Si on the surface. The tailing at the Ni and Pt peak position indicates some roughening of the silicide layer. This could be due to the initially rough state of the crystalline and amorphous interface of the as-deposited Si where some Si grains extend through the whole Si layer (Fig. 1), but this is more probably related to the beginning of inversion. At 700°C, the Ni and Pt signal shows some broadening with a slight increase in the average Si concentration to 60%. At 750°C (Fig. 6c), the silicide layer becomes partially inverted with high Si ratio on the surface and the Ni and Pt distributions are very inhomogeneous. This is in accordance with the large increase in the sheet resistance observed for the

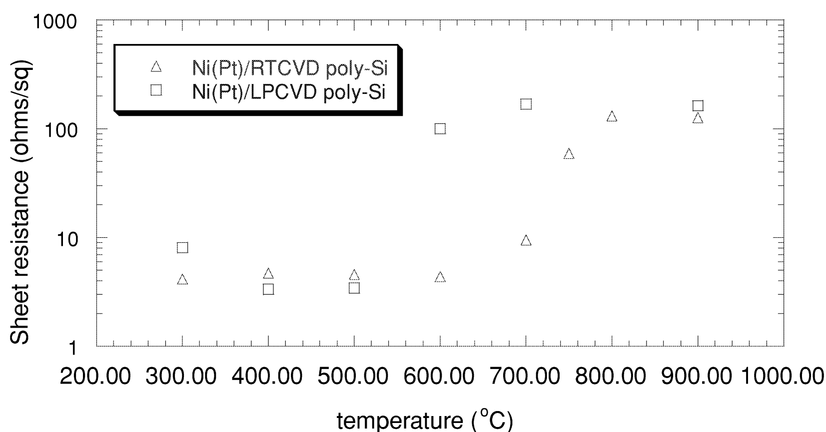

Fig. 5. Sheet resistance of Ni(Pt) on RTCVD-Si and LPCVD poly-Si after annealing at various temperatures.

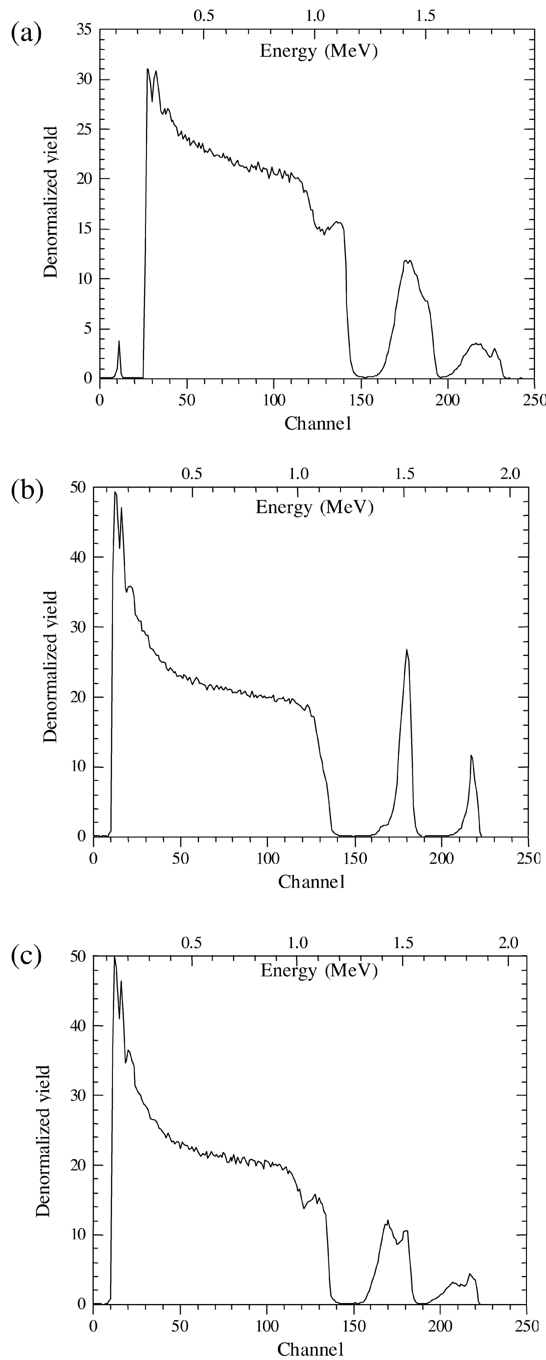

Fig. 6. RBS spectra showing the extent of poly-Si inversion on (a) Ni(Pt)/LPCVD poly-Si at 600°C. (b) Ni(Pt)/RTCVD-Si at 600°C. (c) Ni(Pt)/RTCVD-Si at 750°C.

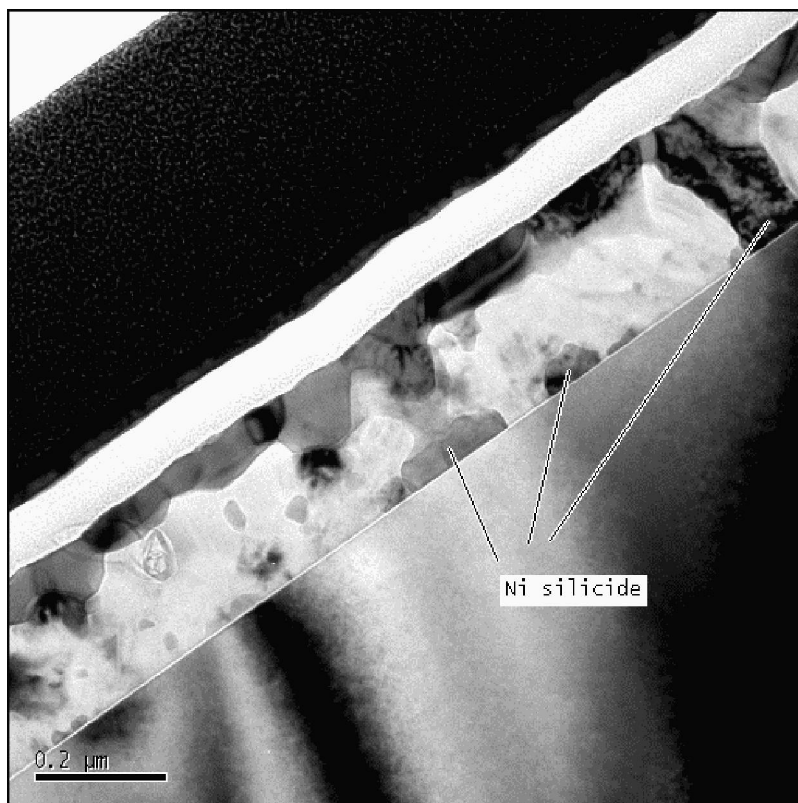

Fig. 7. XTEM micrograph of Ni(Pt) on RTCVD-Si after annealing at 600°C.

RTCVD sample annealed at 750°C. Therefore, the extensive or more complete inversion is only observed at 750°C, which is a relatively higher temperature than the one on the LPCVD sample.

Fig. 7 shows XTEM analysis of the Ni(Pt)Si formed at 600°C on RTCVD-Si. The Ni(Pt)Si layer is rather uniform on the surface with no exposure of Si grains observed. This is in agreement with the RBS results which show no inversion of Ni(Pt) on RTCVD-Si at 600°C. The Si layer is polycrystalline in nature corresponding to the crystallization of the initial as-grown upper layer of amorphous Si in the presence of silicides. The poly-Si grains are relatively large and free of defects. A small amount of silicide can be seen to extend vertically through the Si layer.

4. Discussion

The delayed transformation from NiSi to $NiSi_2$ can be understood in terms of nucleation controlled concept since the formation of $NiSi_2$ on crystalline Si is known to be controlled by nucleation. When the change in free energy (ΔG) of a reaction ($NiSi + Si \rightarrow NiSi_2$) is countered by an increase in interfacial energy associated with the creation of new phase ($\Delta\sigma = \sigma(NiSi_2/Si) + \sigma(NiSi_2/NiSi) - \sigma(NiSi/Si)$), the reaction is nucleation controlled. Under such circumstance, the nucleation activation energy barrier is proportional to $\Delta\sigma^3/\Delta G^2$. Both $\Delta\sigma$ and ΔG may be influenced by the addition of

alloying element. NiSi and PtSi are able to form complete pseudobinary solid solution since they have the same orthorhombic structure and their lattice parameters are within 15%. The presence of Pt in the solid solution of Ni(Pt)Si has resulted in a decrease in Gibbs energy of NiSi [4].

For the case of Ni(Pt) on Si(100) and Si(111), the enhanced stability is attributed to both a decrease in the free energy term due to the formation of a silicide solution and an increase in interfacial energy term associated with a strong tendency to form epitaxial or strongly oriented NiSi on Si [4]. However, for the silicide formation on poly-Si, the strong tendency to form textured Ni(Pt)Si is absent. The Ni(Pt)Si films are polycrystalline in nature. Therefore, the change in Gibbs free energy due to the addition of Pt seems to be a dominant factor in the reduced nucleation rate of $NiSi_2$ and consequently in the stabilization of Ni(Pt)Si on poly-Si (LPCVD) and partial amorphous-Si (RTCVD) substrates.

It was found in the present study that for pure Ni films on LPCVD and RTCVD-Si annealed at 700°C, NiSi phase could not be detected and that the nucleation of $NiSi_2$ has started. This temperature is thus lower than the one observed for nucleation of $NiSi_2$ on the monocrystalline Si (around 750°C). For silicide formation on poly-Si, the thermodynamic driving force should be very similar to that on monocrystalline Si [9]. Although the poly-Si is in a higher energy state than monocrystalline Si, the difference is small compared with the heat of formation of silicides. The Si grain boundary energy is about one order of magnitude smaller than the difference in the heats of formation of NiSi and $NiSi_2$ and two orders of magnitude smaller than the heat of formation of a typical silicide. Therefore, the silicide formation temperature and phase sequence should not be affected by the introduction of poly-Si from the point of view of thermodynamic driving forces. The slightly lower nucleation temperature observed in the poly-Si substrates is probably due to the occurrence of layer inversion, which has generated higher number of nucleation sites at an annealing temperature of 700°C and/or a higher chance for the nuclei to be stabilized during the layer reconstruction. The higher density of nuclei is usually possible near cleavage steps and other substrate imperfections. Layer inversion has been shown to be preceded by plastic deformation [10], this would generate dislocations and stored energy within the crystals. This prompts recrystallization with the presence of abundance of recrystallization nuclei and suggests a high possibility for $NiSi_2$ to be nucleated.

Another possibility that enables an easier $NiSi_2$ nucleation for pure Ni silicidation on poly-Si could be due to a difference in stress state of NiSi on poly-Si compared to single crystal Si. The thermodynamic gain result from the transformation of NiSi to $NiSi_2$ has small chemical ΔGs, variation in stress can possibly modulate the nucleation and/or the lateral propagation of the new phases from discrete nucleation centers [11]. It has been shown that compressive stress appears during the formation of $NiSi_2$ [12]. This might influence the nucleation-controlled formation of $NiSi_2$. On the other hand, in-situ stress measurements have shown that layer inversion led to tensile stress [13]. This tensile stress may compensate the intrinsic compressive stress generated during the formation of $NiSi_2$ so that the nucleation barrier for the disilicide is lowered.

It has been reported that the formation temperature of $NiSi_2$ is considerably reduced on amorphous Si. For example, disilicides of both nickel and cobalt have been formed at low temperatures (about 400°C) on evaporated amorphous silicon (a-Si) films [14]. After annealing at 360°C of Ni films on ion implantation preamorphized Si, the presence of $NiSi_2$ was dominantly found [15]. In these cases, the $NiSi_2$ formation was found to be diffusion controlled which means that the nucleation is not anymore the limiting step. This can be understood considering the additional free energy of a-Si compared to c-Si (heat of crystallization: 10.6 kJ/mol), which increases considerably the formation energy of $NiSi_2$ on a-Si compared to the one on c-Si. This extra driving force may overcome the stress and

surface effects with the result of a lower formation temperature of $NiSi_2$. However, on the RTCVD-Si in this study, which resulted in a partially amorphous Si on the upper layer, $NiSi_2$ was not observed at low temperature. In fact, the formation of NiSi was observed at low temperature from 300°C up to 600°C, indicating that the formation energy of $NiSi_2$ on RTCVD-Si is similar to that on the fully poly-Si case. This result is in accordance with another report where it was found that $NiSi_2$ does not form on ion-amorphized Si layers at low temperature, and heat treatments over 750°C are still required [16]. Formation of $CoSi_2$ at 700°C on amorphous/poly-Si gate stack is another example whereby the disilicide formation temperature is not lowered in the presence of amorphous-Si substrate [17]. This indicates that the different nature of the amorphous-Si may affect the silicide phase formation. It has been suggested that the enhancement of silicide formation with amorphous-Si takes place only when amorphous Si is in the 'as-implanted' state and is due to the heat release during the transformation of Si into a 'relaxed' state, i.e. the decrease of excess free energy stored in the amorphous Si.

The reduction of surface energy and grain boundary energies is the driving force for poly-Si inversion, and should be small. It might thus be affected by some other small changes. However, for the LPCVD samples, the poly-Si inversion behavior is not affected much by the addition of Pt. It has also been shown that Pt layer (1% of Ni) deposited in between Ni and poly-Si has no significant effect on the morphological stability [3]. The fact that the degradation of Ni(Pt)Si on poly-Si occurs at similar temperatures as the ones of NiSi on poly-Si seems to justify that the extent of inversion or degradation mechanism is more dependent on the microstructure of the underlying substrate layer than the nature of the silicide top layer [17].

From the RBS analysis and TEM results, the LPCVD poly-Si is almost fully inverted at temperatures as low as 600°C, whereas on RTCVD-Si, the silicide maintains large coverage on top of the poly-Si at temperatures of 600 and 700°C. This is a little bit surprising in view of the amorphous layer present initially in the RTCVD samples. However, the grain size of Si in the RTCVD sample annealed at 600°C (Fig. 7) was found to be larger than that of the LPCVD sample (not shown). In principle, 'pure' a-Si should not crystallize at these low temperatures but the presence of silicide has been found to reduce the crystallization temperature of a-Si [18]. The recrystallization might have occurred before inversion and results in the enlarged poly-Si grains. The larger poly-Si grains are more stable and are certainly the cause for the lower extent of the layer inversion of the silicide on RTCVD-Si. This further shows that the driving force for the layer inversion is the reduction of the grain boundary energy and surface energy of the underlying poly-Si grains.

In XTEM images, columns of silicides can be seen through the Si substrates grown by RTCVD. This result seems to support the idea that Ni in-diffusion through grain boundaries in the underlying Si is the dominant factor in determining the thermal stability of polycide structure under RTA. Some grain boundaries provide the pipelines for Ni in-diffusion and silicides form along it.

5. Conclusion

In the present study, we observe the enhanced stability of Ni(Pt)Si on poly-Si grown by LPCVD and RTCVD technique. This seems to indicate that for nucleation, the change in Gibbs energy upon alloying with Pt is preponderant compared to interfacial energy term. For pure Ni silicidation, NiSi was not detected at 700°C due to $NiSi_2$ nucleation. This is a lower $NiSi_2$ nucleation temperature

compared to the one on single crystal (750°C). On the partial amorphous Si structure grown by RTCVD, no difference in the Ni–Si phase formation sequence was observed compared to those on complete poly-Si structures grown by LPCVD. The Ni(Pt)Si film shows a better resistance to layer inversion on the RTCVD poly-Si due to larger Si grains after annealing.

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References

[1] F.M. d'Heurle, J. Mater. Res. 3 (1988) 167.
[2] S.R. Das, D.-X. Xu, M. Nourmia, L. Lebrun, A. Naem, Mater. Res. Soc. Symp. Proc. 427 (1996) 541.
[3] S. Nygren, D. Caffin, M. Ostling, F.M. d'Heurle, Appl. Surf. Sci. 53 (1991) 87.
[4] D. Mangelinck, J.Y. Dai, J.S. Pan, S.K. Lahiri, Appl. Phys. Lett. 75 (12) (1999) 1736.
[5] C. Basa, M. Tinani, E.A. Irene, J. Vac. Sci. Technol. A 16 (4) (1998) 2466.
[6] S. Sivaram, in: Chemical Vapor Deposition: Thermal and Plasma Deposition of Electronic Materials, Van Nostrand Reinhold, 1995, p. 235.
[7] S.P. Murarka, J. Vac. Sci. Technol. B 2 (4) (1994) 693.
[8] P.S. Lee, D. Mangelinck, K.L. Pey, Z.X. Shen, J. Ding, T. Osipowicz, A. See, Electrochem. Solid State Lett. 3 (3) (2000) 153.
[9] E. Colgan, J.P. Gambino, Q.Z. Hong, Mater. Sci. Eng. R16 (1996) 43.
[10] Q.Z. Hong, S.Q. Hong, F.M. Heurle, J.M.E. Harper, Thin Solid Films 253 (1994) 479.
[11] F.M. d'Heurle, O. Thomas, Defect Diffusion Forum 129–130 (1996) 137.
[12] C.J. Tsai, K.H. Hu, Thin Solid Films 350 (1999) 91.
[13] Q.Z. Hong, F.M. d'Heurle, J.M.E. Harper, S.Q. Hong, Appl. Phys. Lett. 62 (21) (1993) 2637.
[14] C.-D. Lien, M.-A. Nicolet, S.S. Lau, Phys. Stat. Sol. (a) 81 (1984) 123.
[15] Y.N. Erokhin, F. Hong, S. Pramanick, G.A. Rozgonyi, B.K. Patnaik, C.W. White, Appl. Phys. Lett. 63 (23) (1993) 3173.
[16] B. Mohadjeri, J. Linnros, B.G. Svensson, M. Östling, Phys. Rev. Lett. 68 (12) (1992) 1872.
[17] W.-M. Chen, S.K. Banerjee, J.C. Lee, Appl. Phys. Lett. 64 (12) (1994) 1505.
[18] S.Y. Yoon, S.J. Park, K.H. Kim, J. Jang, C.O. Kim, J. Appl. Phys. 87 (1) (2000) 609.