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Interface strain study of thin Lu_2O_3/Si using HRBS

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Abstract

The interface of thin Lu_2O_3 on silicon has been studied using high-resolution RBS (HRBS) for samples annealed at different temperatures. Thin rare earth metal oxides are of interest as candidates for next generation transistor gate dielectrics, due to their high-*k* values allowing for equivalent oxide thickness (EOT) of less than 1 nm. Among them, Lu_2O_3 has been found to have the highest lattice energy and largest band gap, making it a good candidate for an alternative high-*k* gate dielectric. HRBS depth profiling results have shown the existence of a thin (~2 nm) transitional silicate layer beneath the Lu_2O_3 films. The thicknesses of the Lu_2O_3 films were found to be ~8 nm and the films were determined to be non-crystalline. Angular scans were performed across the [1 1 0] and [1 1 1] axis along planar channels, and clear shifts in the channeling minimum indicate the presence of Si lattice strain at the silicate/Si interface.

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Keywords: High-resolution RBS; Interfacial strain; Lu_2O_3 thin films; Channeling

1. Introduction

The demand for faster devices with higher speed and lower power consumption has motivated the rapid downscaling of metal-oxide semiconductor field effect transistors (MOSFETs). The physical dimensions of MOSFETs have been reduced to the stage where the required SiO_2 gate dielectric thickness is now less than 1 nm. Silicon oxide of such thickness can no longer serve as the gate dielectric, due to the unacceptable levels of direct tunneling current through the layer (gate leakage current). Intense research is presently ongoing to find suitable alternative "high-*k*" gate dielectrics with higher dielectric constants and equivalent-oxide-thickness (EOT) of less than 1 nm. Many possible systems are currently being studied [1]: Si_3N_4, HfO_2, Al_2O_3, La_2O_3 etc. In particular, a 1.2 nm thick SiON layer is currently used as the gate dielectric for Intel's 35 nm gate length CMOS technology [2]. Recently, quantum mechanical calculations of gate leakage current using a semi-empirical model based on the WKB approximation have shown that lanthanide based oxides La_2O_3 seem to have the lowest EOT scaling limit as compared to various candidates [3]. Among the Lanthanide oxides, Lu_2O_3 shows strong potential as it has the highest lattice energy and band gap [4]. It is therefore of interest to study the suitability of Lu_2O_3 as the next-generation gate dielectric. One of the important factors that determine the suitability of any gate dielectric is the strain exerted by the dielectric on the Si channel below it, which will affect the charge mobility along the channel.

In cases where the thickness of the Lu_2O_3 thin films being less than 10 nm, conventional RBS with a depth resolution in the order of 10 nm is not able to provide well resolved depth profiles of the stoichiometry and strain-depth profiling at the film–substrate interface. The HRBS facility at the Centre for Ion Beam Application (CIBA) at the National University of Singapore is capable of sub-nanometer depth resolution if a glancing scattering geometry is used [5]. Recently, HRBS analyses have been

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performed on thin SiO_xN_y [6,7], HfO_2 [8,9] and SiO_2 [10] films on silicon substrates. In this paper, we present the results of the interfacial depth profiling and strain measurements performed on ultra-thin Lu_2O_3/Si interface using HRBS.

2. Experimental

The Lu_2O_3 ultrathin films were deposited directly on p-type (100) Si substrate using the pulse laser deposition (PLD) technique at a base pressure of 4.5×10^{-7} Torr. A KrF excimer-type laser with a wavelength of 248 nm and an energy density of 1.5 J/cm^2 was used. The frequency of the laser was set to 5 Hz. The Si substrates were first cleaned using standard cleaning SC1 and SC2 solutions of Radio Corporation of America (RCA), and then dipped in a 1% HF solution to remove the native oxide. The substrates were loaded immediately after the cleaning step to minimize the SiO_x formation. The samples were subjected to rapid thermal anneal (RTA) after deposition at temperatures ranging from 400 °C to 800 °C for 1 min in oxygen ambient. The annealing step is necessary to test the stability of the film at high temperature. The samples were then measured using a 500 keV He^+ beam which was collimated to 2×2 mm^2 size with a divergence angle of less than 1 mrad. The beam was incident on the Lu_2O_3/Si sample which was mounted on a high precision 5-axis goniometer within a UHV scattering chamber. Ions scattered at 65° were analyzed by a 90° sector magnet and were collected by a 100-mm long focal plane detector, which consists of a micro-channel plate (MCP) stacked on a 1-D position sensitive detector placed at the focal plane of the spectrometer. Non-aligned (random) HRBS spectra of these samples were measured at a sample tilt of 40°, which were then simulated and fitted using the SIMNRA program to obtain the elemental depth profiles. Angular scans across the [111] channeling direction along the (110) plane were also performed to measure the Si interfacial lattice strain.

3. Results and discussion

3.1. Depth profiling

Fig. 1 shows the measured and simulated random spectra of the as-deposited Lu_2O_3/Si sample and the 600 °C annealed samples. The spectra were first processed by correcting for the non-linear gain variation along the length of the MCP, and a low-level linear background was then sub-

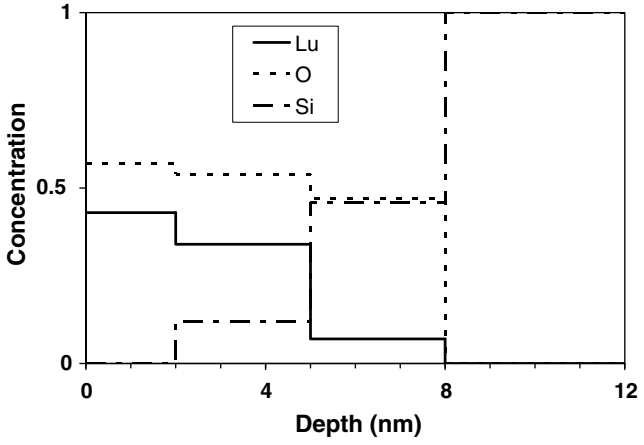

Fig. 2a. The elemental depth profile of the as-deposited sample.

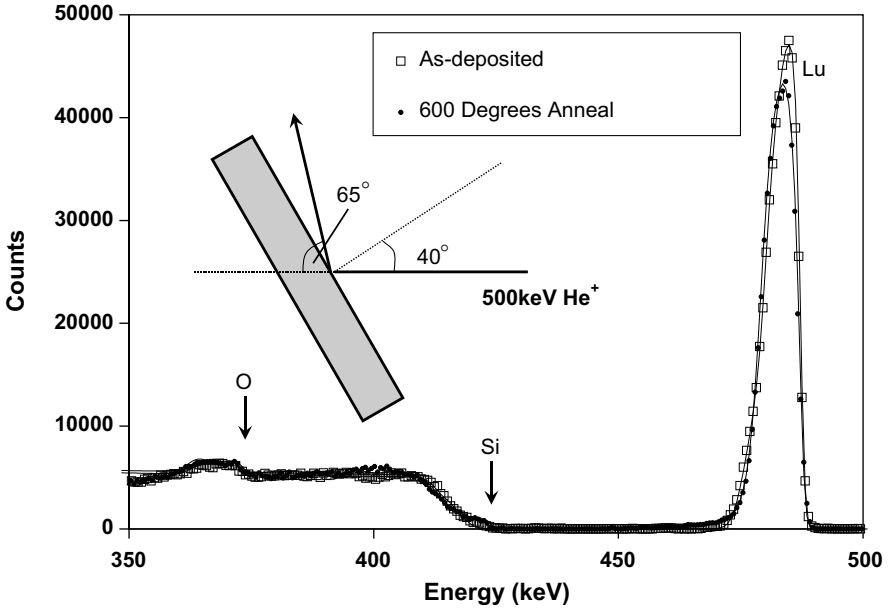

Fig. 1. Random HRBS spectrum of the as-deposited and 600 °C – annealed sample, measured at a scattering of 65°. 500 keV ions were incident with sample tilt of 40°. The simulated curve (solid line) indicates a total film thickness of ~5 nm and a ~3 nm interfacial SiO_x layer. The low energy tail of the Lu signal indicates the diffusion of Lu atoms into the substrate.

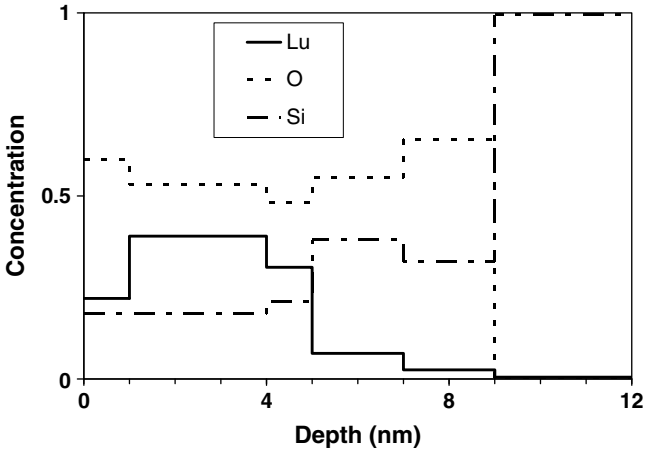

Fig. 2b. The elemental depth profile of the 600 °C annealed sample. The silicate layer thickness has increased after anneal, and Si atoms are found on the surface.

tracted. The surface energies of Lu and O signals are at ~487 keV and ~373 keV, respectively. The gradual slope of low-energy edge of the Lu signals and in the leading edge of the Si signals indicate the presence of a rough Lu silicate interface layer, while the shift in the Si signal indicates the presence of a thin SiO_x layer. The spectrum of the 600 °C – annealed sample suggests that Lu has diffused into the substrate, due to the low energy tail at the low energy part of the Lu signal. The surface of the as-deposited sample is a Lu_2O_3 layer with no Si intermixing, while Si is present at the surface after anneal.

The spectra were fitted using the SIMNRA simulation software, and the elemental depth profiles for the Lu thin film were derived directly from a target layer structure that fits the data. The film depth profiles are shown in Fig. 2(a) for the as-deposited sample and Fig. 2(b) for the 600 °C

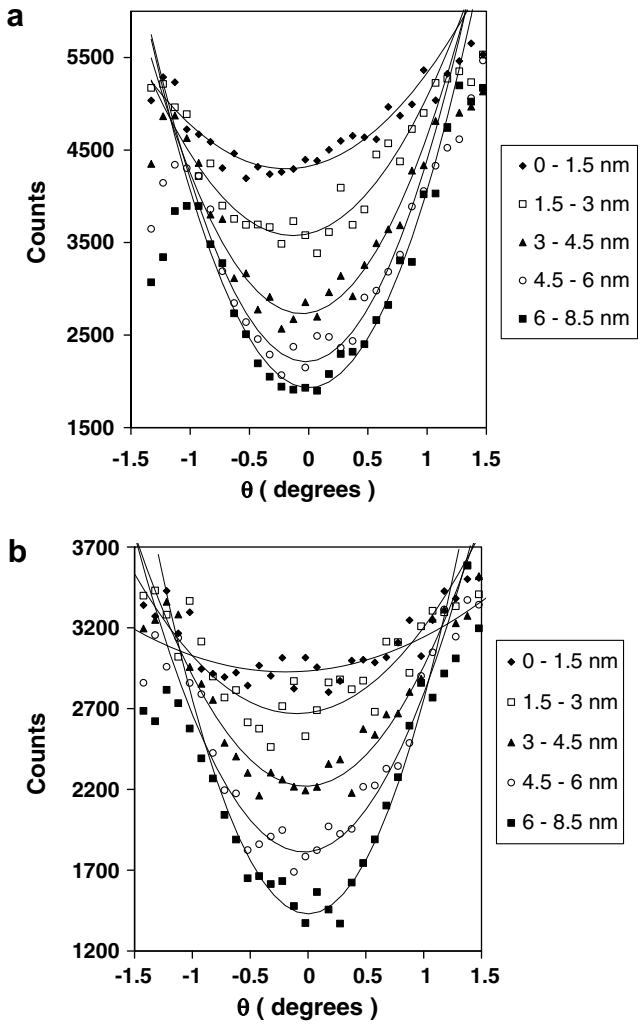

Fig. 3. (a) and (b) Angular scan for the as-deposited and the 400 °C annealed sample. The as-deposited sample shows a strained Si lattice, which relaxes with annealing.

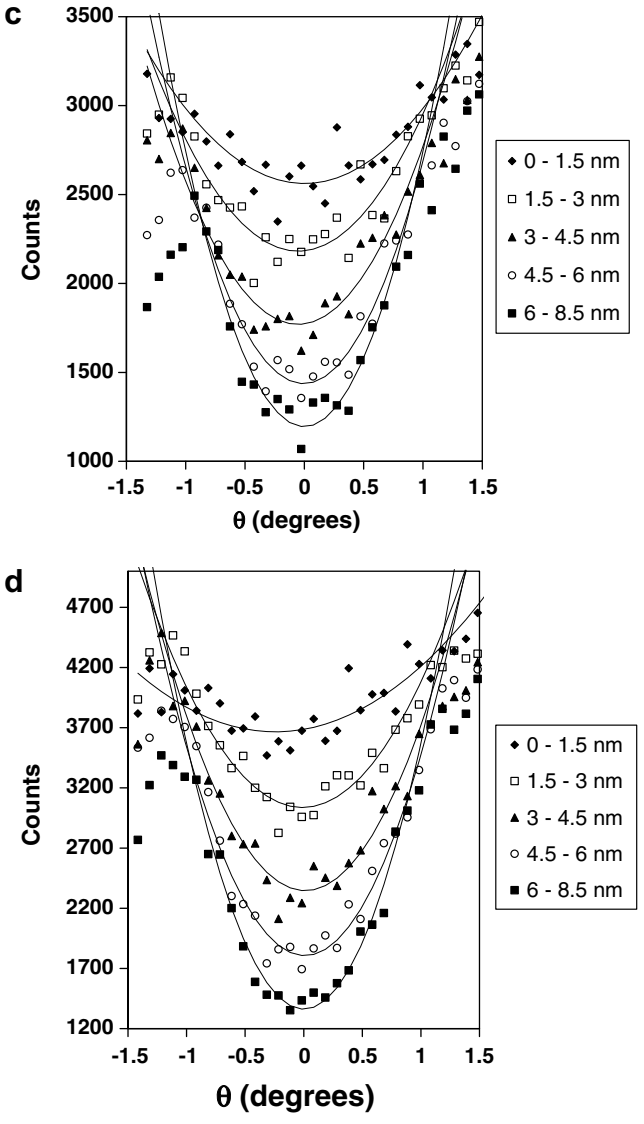

Fig. 3. (c) and (d) Angular scan for the 600 °C and the 800 °C annealed sample. The lattice strain in the decreases with higher annealing temperatures, so that at 800 °C the lattice strain is below detection limit.

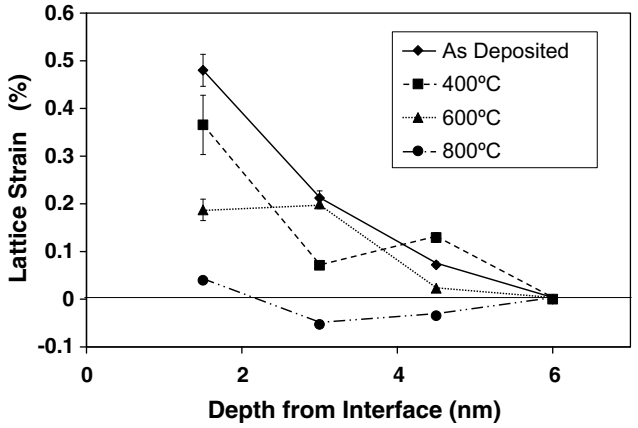

Fig. 4. The variation of lattice strain (%) versus depth from interface. The lattice strain at the interface decreases with increasing annealing temperature.

annealed sample. The uncertainties of the elemental depth profiles may arise from the error in the fit, beam straggling, as well as the counting statistics. For Lu at the surface, the combined error is expected to be ~0.5%, and this error will be expected to increase with depth due to straggling. For all samples, an interfacial SiO_x film exists at the interface with the Si substrate.

3.2. Interfacial strain measurement

Angular scans were performed on the as-deposited sample, and samples annealed at 400 °C, 600 °C, and 800 °C in order to measure the lattice strain of Si. The Si signal in the HRBS spectra measured at fixed angular positions along the (1 1 0) plane across the [1 1 1] direction is divided into 5 consecutive narrow strips at the film–substrate interface, corresponding to linear widths of 1.5 nm each. The total yield of each strip is plotted as a function of incident angle relative to the [1 1 1] direction, and strips at different depth from the film–substrate interface are plotted together for each of the four samples in Fig. 3(a)–(d). The strip on the thin film side of the interface shows no channeling dip, while the strip on the substrate side of the interface shows a well-defined dip. Each set of data is then fitted with a second-order polynomial, and the minimum of each fit indicates the position of the corresponding dip.

Results indicate a shift in the [1 1 1] channeling dip towards smaller incident angles with decreasing depth from the interface. This indicates a local tensile stress at the interface up to a depth of ~6 nm within the Si substrate as measured from the interface. The magnitude of the dip shift is the largest in the as-deposited sample, indicating a lattice strain of about 0.5% as estimated by $\varepsilon = 2\Delta\theta_i \operatorname{cosec}(2\theta_i)$, where $\Delta\theta_i$ is the angular shift of the channeling dip, and θ_i is the angular position of the [1 1 1] axis. The variation of strain versus depth is shown in Fig. 4. This strain decreases in magnitude in samples with increasing annealing temperature, so that the lattice strain of 800 °C annealed sample has fallen below the detection limit of 0.1%. This strain extends up to ~6 nm from the interface, which will significantly affect the charge carrier mobility in the inversion layer in MOSFETs, if Lu_2O_3 were to be used as a gate dielectric.

4. Conclusion

High-resolution RBS has been used to conduct elemental depth profiling and Si lattice strain-depth profiling on Lu_2O_3 thin films deposited on Si using PLD. A rough silicate layer exists above a thin SiO_x layer for all films, and the thickness of the silicate layer increases after annealing. Angular scans across the [1 1 1] axis along the (1 1 0) plane have been conducted to measure the lattice strain of Si at the film interface. Dip shifts towards smaller angles were observed, indicating that the Si lattice is under vertical tensile strain at the film interface. The lattice strain decreases with increasing annealing temperature, the as-deposited sample shows a lattice strain of ~0.5%, which decreases in samples annealed at increasing temperature.

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