Lanthanide-based graded barrier structure for enhanced nanocrystal memory properties

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A memory structure comprising Ge nanocrystals and lanthanide-based charge trapping dielectric stack was fabricated to realize a self-aligned graded barrier structure. By exploiting efficient charge trapping of the nanocrystals embedded in the heterogeneous high-*k* dielectric, strong memory effect was manifested by a large counterclockwise capacitance-voltage hysteresis of 2.7 V under a low voltage operation of ±4 V. The high-*k* barrier with graded composition provides a favorable confinement barrier for improved hole retention with simultaneous enlargement of the memory window. © *2009 American Institute of Physics*. [doi:10.1063/1.3224188]

Studies on alternative structures and materials for nonvolatile memory (NVM) device have recently attracted much attention in order to meet the scaling requirements of conventional flash memory. Attention has recently focused on charge trap memory devices utilizing nitride layer or nanocrystals as charge storage elements.[1–3] The discreteness of the charge traps makes it more robust to stress-induced leakage current, which allows further dielectric scaling. Although semiconductor nanocrystal-based memory is a promising candidate for future NVMs, it suffers from weak electrostatic coupling and small memory window (threshold voltage shift).[4,5] In this regard, the use of alternative materials as the nanocrystal floating gate[6,7] and the implementation of different high-*k* dielectric materials have been explored.[8–11] However, the tradeoff between program/erase efficiency and data retention remains an important issue. Recent efforts to obtain an optimum compromise of the memory performance involve band gap engineering of the tunnel oxide comprising SiO_2/HfO_2 bilayer tunnel dielectric,[6,12,13] $Si_3N_4/SiO_2/Si_3N_4$ crested tunnel barrier,[14] and $Al_2O_3/HfO_2/Al_2O_3$ trilayer tunnel oxide.[7] However, the realization of a good interface quality between the multilayer dielectric is difficult and possible interface charge trapping could degrade the device performance.

In this work, we have demonstrated a self-aligned graded barrier structure formation for simultaneous improvement in the memory window and charge retention behavior. Charge trapping effect of a Ge nanocrystal-based memory device utilizing Lu_2O_3 as the tunneling dielectric and Al_2O_3 control dielectric can be found in our previous work.[11] This communication presents an approach to achieve enhanced memory performance with a gradual change in layer composition due to thermally induced intermixing of oxide components. The graded high-*k* barrier with Ge nanocrystal charge trapping scheme provides great potential for achieving a large threshold voltage window under low operation voltage with simultaneous improvement in the retention behavior.

P-type (100) Si substrates were prepared by standard Radio Corporation of American clean followed by HF (1%) native oxide removal. A simple pulsed laser deposition technique was utilized for the dielectric film deposition and nanocrystal fabrication. A 248 nm KrF pulsed laser was used to ablate the target assembly illustrated in the previous work[10] in a high vacuum system (modified by Quasi-S Pte. Ltd.) at room temperature. ~3-nm-thick Lu_2O_3 tunneling oxide layer was deposited, followed by ~9 nm Ge nanocrystals embedded in Lu_2O_3 with the laser beam vaporizing the two component materials alternately. An Al_2O_3 capping layer (~5 nm) was deposited by ablating a round Al_2O_3 (99.999%) target (diameter $D=25$ mm) to form an effective blocking oxide. After deposition, the dielectric film stack was subjected to rapid thermal anneal at 400 and 800 °C for 60 s in N_2 ambient. A control sample was also fabricated under the same conditions without Ge incorporation.

The Rutherford backscattering spectra (RBS) were obtained for the film compositional analysis using 650 keV He^+ ions at a scattering angle of 65° and an incident angle of 60°. Metal-insulator-semiconductor (MIS) memory capacitor structures were fabricated by evaporating Au top electrodes with 0.3 mm diameter and backside electrodes of ~500 nm thick after native oxide removal. The memory behavior was investigated by performing capacitance-voltage (*C-V*) measurements at room temperature using HP4284A precision *LCR* meter.

Figure 1(a) shows the cross-sectional transmission electron microscopy (TEM) image of the 800 °C annealed lanthanide-based high-*k* dielectric stack with Ge nanocrystals sandwiched between the Lu-based tunnel oxide and aluminum-based control oxide. Figure inset shows the schematic illustration of the MIS capacitor device structure fabricated for memory characterization. The planar TEM image of the Ge nanocrystals embedded in Lu_2O_3/Al_2O_3 dielectric stack is shown in Fig. 1(b). Nearly spherical-shaped nanocrystals with a high areal density of 9×10^{11} cm^{-2} and a size range of ~3–8 nm was observed in the amorphous Lu_2O_3 matrix. The figure inset shows the lattice fringes of 0.32 nm indicating single crystalline state of a (111) Ge nanocrystal

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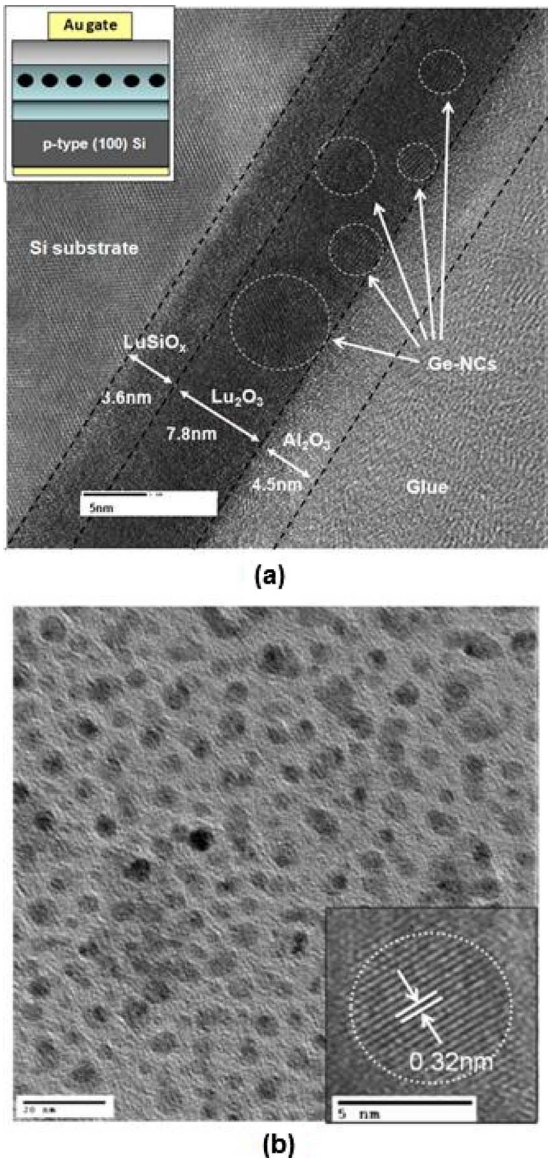

FIG. 1. (Color online) (a) Cross-sectional TEM image of the Ge nanocrystals embedded in the amorphous $LuSiO_x/Lu_2O_3/Al_2O_3$ film stack after annealing at 800 °C. Figure inset shows the schematic illustration of the device structure and (b) planar TEM image of the Ge nanocrystals embedded in the film. Figure inset shows the high resolution image of a single crystalline Ge nanocrystal.

of ~6 nm in diameter. The Ge nanocrystals can also be formed at 400 °C annealing temperature and the formation mechanism has been previously discussed in Ref. 13. No significant changes in the nanocrystal size and density was obtained under a higher annealing temperature, although a small degree of coalescence was observed and associated with enhanced diffusion of Ge atoms. The formation of lanthanide-based graded barrier is shown from the RBS spectrum of the dielectric film stack annealed at 800 °C in Fig. 2. Curve fitting (using SIMNRA software) result reveals the formation of compositionally graded dielectric stack with Lu-silicate and SiO_x interfacial layer after the annealing treatment. The interdiffusion of Si, Ge, Lu, and Al atoms promotes the intermixing of film components that forms the resultant lanthanide-based high-k stack with gradual change in layer composition.

Figure 3(a) shows the high-frequency (100 kHz) C-V characteristics obtained by performing bidirectional bias

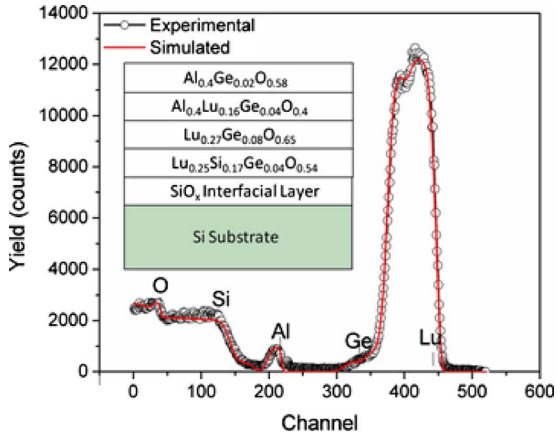

FIG. 2. (Color online) RBS spectra for the 800 °C annealed gate dielectric stack with the curve fitted using SIMNRA 6.03 for the evaluation of compositional depth distributions.

sweeps on the 400 and 800 °C annealed memory capacitor devices and the control device without nanocrystals. An enlarged memory window with a significant flatband voltage shift (ΔV_{FB}) of 2.7 V was obtained under a low operation voltage of ±4 V, indicating a large increase in charge storage capability as compared to the ΔV_{FB} of 1.3 V for the 400 °C annealed device. The C-V curve of the reference sample without Ge incorporation exhibits a relatively small hysteresis (~0.2 V) related to oxide or interface states tapping effect. Hence the major charge storage effect from the device with Ge nanocrystals is attributed to the trapped

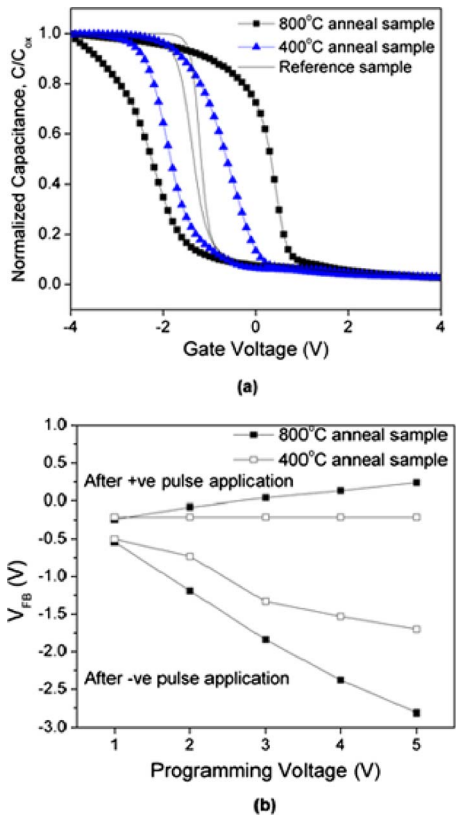

FIG. 3. (Color online) (a) High-frequency (100 kHz) capacitance-voltage (C-V) of the MIS memory capacitor device annealed at 400 and 800 °C plotted together with the reference curve without Ge and (b) flatband voltage of the 400 and 800 °C annealed devices measured after applying sequential increasing programming pulse voltages for 1 s.

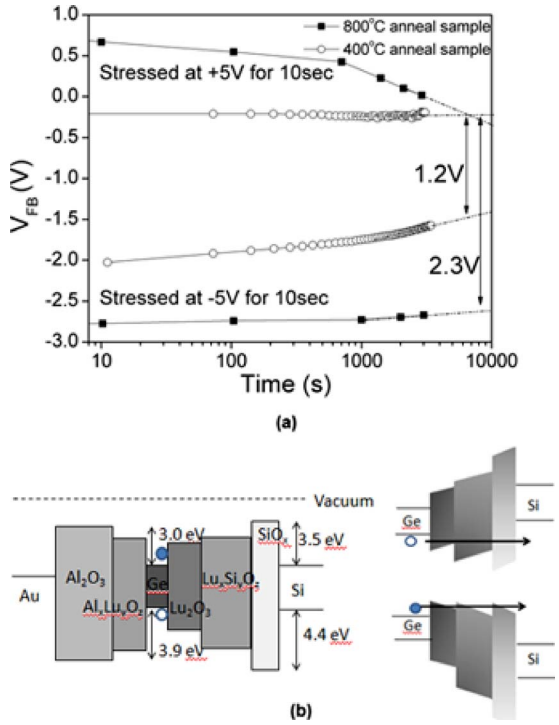

FIG. 4. (Color online) (a) Retention characteristics of the 400 and 800 °C annealed memory capacitor device after applying positive and negative stress voltages of ±5 V for 10 s at room temperature and (b) schematic energy band diagram of the memory capacitor device structure comprising Ge nanocrystals sandwiched between $SiO_x/Lu_xSi_yO_z/Lu_2O_3$ tunnel dielectric and $Al_xLu_yO_z/Al_2O_3$ control dielectric stack under flatband condition; and illustration of electron (solid circle) and hole (open circle) discharging path through the tunnel dielectric stack under retention mode.

charges in the nanocrystals. Since no significant difference in nanocrystal size and density was observed between samples annealed at 400 and 800 °C, the improved memory behavior is associated to the modifications of charge injection properties across the graded barrier structure. In addition, a larger amount of charge trapping sites are available with different nature of trapping centers created between Ge and the surrounding Lu-based high-*k* dielectric matrix comprising $Lu_xSi_yO_z$, Lu_2O_3, and $Al_xLu_yO_z$. The charge storage behavior of the device was further investigated by performing *C-V* sweeps after applying varying pulse amplitude for 1 s. Figure 3(b) shows the measured programming characteristics of the device, with the measured V_{FB} plotted as a function of the applied programming voltages. Significant ΔV_{FB} from −0.96 to −2.56 V was obtained with increasing negative programming voltages from −2 to −5 V with respect to the quasineutral *C-V* curve. The large programming efficiency obtained with hole injection initiated at a low charging voltage of −2 V suggests dominant direct tunneling contribution through the SiO_x interfacial layer on the charging behavior. On the other hand, a smaller charging efficiency observed from the 400 °C sample is related to a smaller Fowler–Nordheim tunneling current through the single-layer Lu_2O_3 tunnel oxide.[12]

Retention characteristics of the memory devices after 400 and 800 °C annealing are shown in Fig. 4(a), after performing positive and negative stress voltages of ±5 V for 10 s at room temperature. A large memory window of 2.3 V was retained for the 800 °C annealed sample after a holding time of 10^4 s. A faster charge storage loss was observed after applying positive stress voltage, indicating a higher electron loss rate due to a higher conduction band edge of the Ge nanocrystal.[15] By considering solely the retention time of the trapped holes, a hole decay rate of 0.05 V/decade was obtained for the 800 °C anneal sample. This shows a significant improvement in hole-based retention, as compared to a hole decay rate of 0.21 V/decade for the 400 °C anneal sample. The improved retention suggests a favorable band alignment for charge confinement, as depicted from the illustration of band profile in Fig. 4(b). The energy band profile between the Ge nanocrystals and Si substrate is used to illustrate hole and electron discharging through the $SiO_x/Lu_xSi_yO_z/Lu_2O_3$ tunnel dielectric stack under retention mode. The higher conduction band edge of Ge results in faster electron discharging through the dielectric. The improved hole retention in the Ge nanocrystals is apparent with a large valence band offset and thick dielectric stack barrier for effective hole confinement. The program/erase cycling characteristics was also evaluated, with minimal voltage shift of 0.1 V observed up to 10^5 write/erase cycles of ±4 V, 100 ms gate disturbs, indicating negligible degradation of the memory window due to stable charge trapping properties under low bias stress application.

In summary, this work presents the promising potential of the memory structure composed of Ge nanocrystals and graded lanthanide-based high-*k* barrier enabled by thermally induced changes in the film composition. Due to an asymmetric structure for favorable band alignment during retention and programming, a simultaneous improvement in charge retention and write/erase behavior was achieved. The results outline the significant role of barrier modification, which provides an enhanced memory behavior with large memory window, low operation voltage, and data nonvolatility.

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