Future Prospects for Silicon Photonics

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ABSTRACT

The field of Silicon Photonics has gained a significant amount of momentum in recent years. Announcements of high speed modulators and cost-efficient light sources in the Silicon-on-insulator material system have helped to make Silicon Photonics a viable contender as a low-cost active photonic platform. As a pioneer in the field, the University of Surrey continues to investigate the prospects of silicon photonics. Herein we present a summary of our work on several key areas such as ion implanted grating devices, high-speed modulators, switches and ring resonators. We conclude with a discussion on an advanced fabrication technique, proton beam writing.

Keywords: Silicon Photonics, modulator, ring resonator, TIR switch, ion implanted grating, proton beam writing

1. INTRODUCTION

Silicon Photonics has gained much attention recently as a viable competitor to copper in high-speed optical interconnects and telecommunications transceivers [1, 2]. There have also been several high profile successes in device and technology development in terms of integrated optical receivers [1], hybrid light sources [3], and high-speed modulation [4] all utilizing the Silicon-On-Insulator (SOI) material platform. As a result, the optical age of silicon may have finally arrived. Because of its high index of refraction coupled with decades of material science research, silicon has the means to provide a basis for photonic circuits that have a high degree of packing density thus resulting in lower overall component costs. Coupled with the ability to integrate high-speed electronic components on the same substrate, Silicon Photonics becomes a contender for telecommunications on the board-to-board level as well as for large area networks.

In some ways the field of Silicon Photonics is actually a relatively mature field in that it has been studied for nearly twenty years [5]. The University of Surrey was one of the first institutions to address some of the earliest issues such as waveguide loss and passive component behavior [6]. This work has continued over the last two decades and is still a very active topic at Surrey. While many technical hurdles have been overcome, there are still many areas where improvements can be made. Herein we discuss several key areas that we are actively investigating. In as many instances as possible, we strive to find polarization independent solutions in so keeping with our belief that these devices are the best way forward in terms of space and effort [7, 8]. We begin with a summary on our grating device work. Grating devices can serve many applications, from filtering to allowing for low-loss fiber/waveguide connections. High-speed switching and modulation methods using CMOS compatible fabrication methods are discussed next. We continue with a discussion of our work on ring resonator devices. Finally, we conclude with a discussion of our current efforts to investigate the advanced fabrication technique of proton beam writing.

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2. GRATING DEVICES

2.1. Dual Grating Assisted Directional Couplers (DGADC)

Devices with smaller waveguide cross-sectional dimensions allow for greater packing density. They also tend to have better performance characteristics such as a larger Free Spectral Range for a ring resonator device [9]. However this move to smaller devices makes coupling of light to/from the circuit very difficult, particularly to/from standard optical fibers that typically have a core dimension of ~ 9 µm. The direct coupling of the fiber to a single mode strip silicon waveguide results in high coupling losses (≈20 dB) due to very different thicknesses and refractive indices. Consequently, several approaches have been proposed for efficient coupling to/from the silicon photonic circuit, the most popular being tapers and grating based couplers [10-12].

We have developed another coupling solution we term the Dual Grating-Assisted Directional Coupler (DGADC) [13]. A schematic of an example design is shown in Figure 1. The top waveguide layer is 5 µm thick with refractive index close to the refractive index of optical fiber, resulting in low insertion loss from the fiber to this waveguide. Therefore a fiber could be butt coupled to the thick SiON waveguide and subsequently the light coupled to the Si_3N_4 waveguide using the first grating, and subsequently to the thin SOI waveguide via the second grating. The silicon nitride waveguide is crucial for the operation of the device, because it enables highly efficient coupling at both gratings, consequently forming an efficient DGADC. This waveguide bridges the gap between SiON and Si layers in both refractive index and thickness. The buried oxide layer serves as the lower cladding layer, for isolation from the substrate, hence removing any leakage loss.

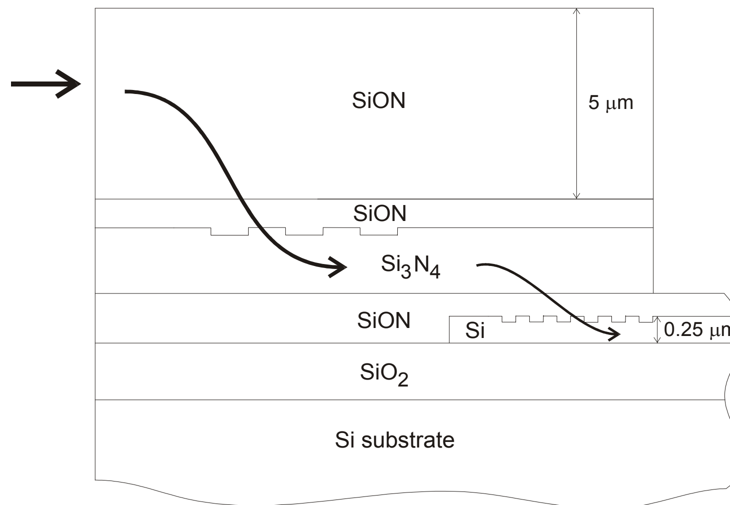


Figure 1. A cross-sectional schematic of a DGADC [13]

Theoretical coupling efficiency is in excess of 90%, while the best measured value to date is 55% [14]. As the thickness of the top SiON layer was not optimized for devices that were fabricated, it is expected that the experimental value for optimized devices can be significantly higher (~ 80%). Typical output of a double DGADC configuration is shown in Figure 2. It can be seen that the resonant peak is well defined with typical side lobe suppression of ~15 dB and bandwidth of ~ 5 nm. Light from an optical fiber was coupled to a 230 nm thick SOI waveguide via the first DGADC and then coupled back to another fiber via the second DGADC. For different grating periods, the resonant peak can be shifted towards longer or shorter wavelengths still achieving coupling efficiency > 42% for both C and L wavelength bands. The spectrum of the devices can be broadened by grating chirping and by varying the duty cycle of the gratings.

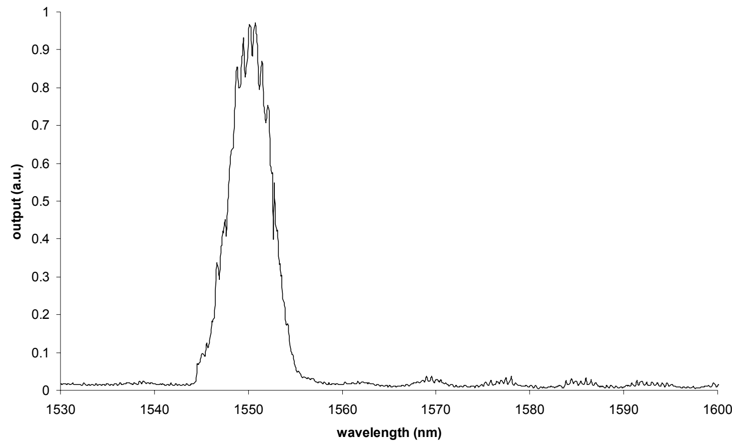


Figure 2. Experimental spectral response of a typical DGADC

2.2. Gratings by Implantation

The University of Surrey is home to one of the premiere ion implantation facilities in the world, the Surrey Ion Beam Centre [15]. We have attempted to utilize this asset by investigating ion implanted gratings. The gratings are formed by first depositing a hard mask (SiN) on top of an SOI wafer with an overlayer thickness of 1.5 μm. E-beam lithography is used to pattern the hard mask. After etching the hard mask, the sample is implanted with O^+ ions at energies of 10 keV and 20 keV to create a more uniform implantation as a function of depth in the SOI. According to a SUSPRE model of the system, the grating depth corresponds to 140 nm [16]. A periodicity of 228 nm with a mark-space ratio of unity was used to give a first order grating response. The end facets of these planar waveguides were then polished and a free-space testing configuration as used in [17] to test ring resonators was used to measure the grating spectral response. The resultant spectral scans were normalized to an identical spectral scan of the chip in a region where the grating was not present. The normalized results are presented in Figure 3 for TE and TM polarizations.

The results demonstrate an attenuation of approximately 10 dB and 6 dB for TE and TM polarizations respectively. The full-width at half-maximum of both polarization states was less than 1nm. While these results show promise for using implants to make gratings, there is still much to be done. These results were obtained on un-annealed samples so the response is most likely due to the change in the index of refraction due to the implantation damage. Nonetheless, the observed attenuation values demonstrate that this method of producing grating structures may have some significant benefits.

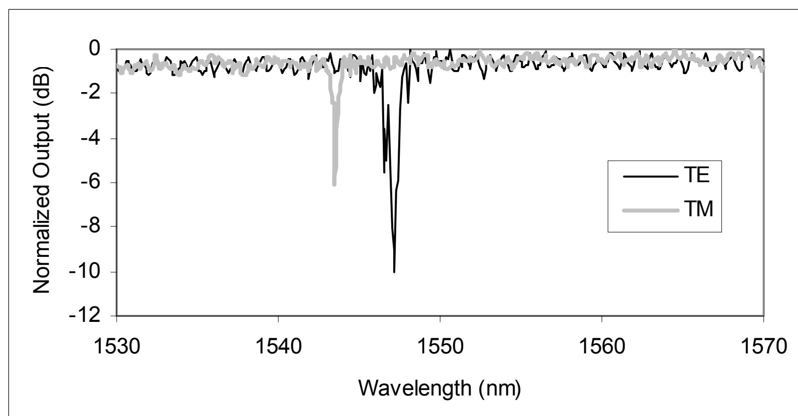


Figure 3. The spectral response of an ion implanted Bragg grating

3. MODULATORS AND SWITCHES

3.1. Modulators

Optical modulation in silicon has been an area of interest at Surrey for more than a decade [18-22]. In fact the first model of a GHz silicon optical modulator was developed here [23]. In keeping with tradition we have developed models for even higher speed modulators based upon carrier depletion in contrast to the carrier injection or capacitive-based methods of earlier modulators [23, 24]. As a further enhancement we have also addressed the issue of polarization dependency and have developed a modulator which is not only high-speed, but also polarization independent. A summary of this modulator is discussed below.

The use of carrier depletion modulators using a p-n junction is a viable solution for increased bandwidths in Silicon Photonics as the speed is not limited by the minority carrier lifetime [25]. The drawback of this method is that the length required to achieve a π-phase shift in a rib waveguide is of the order of millimeters [26]. In order to minimize their size and thereby increase the device packing density, the efficiency of these devices needs to be improved. The solution could be to use smaller waveguide size as proposed in [26], where the confinement of the mode in a submicron waveguide improves the efficiency of the modulator. The issues with submicron waveguides are: the need for efficient optical coupling, higher propagation loss due to surface roughness and increased fabrication tolerances. We attempt to overcome these issues by inserting a p-n junction in a micrometer-sized waveguide whose dimensions were found to give polarization independent characteristics [7]. These dimensions are, waveguide height 1.35 µm, rib width 1µm and etch depth 0.83 µm. The proposed modulator is a p-n junction formed by a V-groove structure, as shown in figure 4. The V-groove junction was created with an angle of 54.7° corresponding the anisotropic etch angle of silicon [18]. A horizontal, flat p-n junction structure was also modeled for the sake of comparison [27]. The optical modeling of the waveguide was the first step in the study of the modulator.

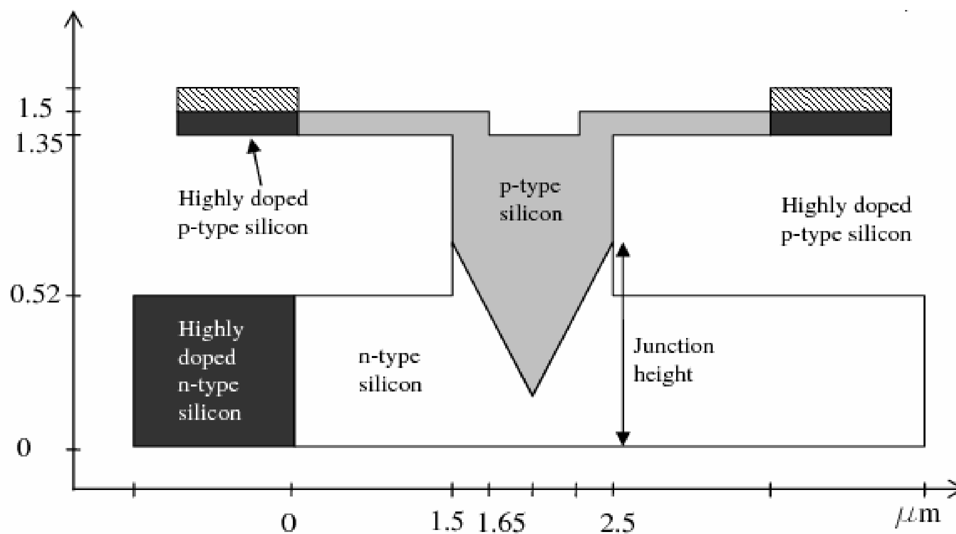


Figure 4. Waveguide cross-section of a V-shaped p-n junction modulator.

3.1.1. Optical Modeling

The flat and V-groove modulator devices were optically modeled using a full-vectorial optical mode solver. This was done in order to determine the necessary dimensions for a birefringence-free, single mode waveguide. The active modulator is then modeled by entering the index change due to the carrier distribution into the mode solver. The index

change is determined by the absorption of light due to free carriers as discussed in the electrical modeling section of this paper, section 3.1.2. From the index change it is possible to determine the optimum device length in order to obtain a π-phase shift [28]. The same method has been used to characterize the transient optical behavior of the modulator. The carrier concentration changes at any given applied bias are introduced into the mode solver for different transient times. The results predict the dynamic change in effective refractive index. Thus a time-dependent π-phase shift as a function of device length can be determined using the same equation that was employed for the DC bias condition.

3.1.2. Electrical modeling

The devices were modeled for both their static and dynamic behavior using Atlas, the device simulation package from Silvaco [29]. The Atlas device simulation predicts the DC bias and time dependent electrical behavior of semiconductor devices. The free carrier profile is determined by Atlas. This profile is then converted into a corresponding refractive index profile using the expressions determined by Soref and Bennett [30]. To determine the voltage associated with a π-phase shift, the change in concentration of free carriers must be known. Assuming a non-uniform change in refractive index, the approximate active device length required to produce the refractive index change associated with a π-phase shift is obtained from the change in effective index. The critical parameters used in the model are provided in Table 1.

Table 1. The electrical simulation parameters of the V-groove modulator

Note: Surfaces of the waveguides are passivated with SiO_2	
Hole carrier lifetime	300 ns
Electron carrier lifetime	700 ns
Si background carrier concentration	1×10^{15} ions/cm3
P-type silicon	1×10^{18} ions/cm3
N-type silicon	1×10^{18} ions/cm3
Resistive contact P^+ and N^+	1×10^{19} ions/cm3

3.1.3. Efficiency of the modulator and positioning of the junction inside the waveguide

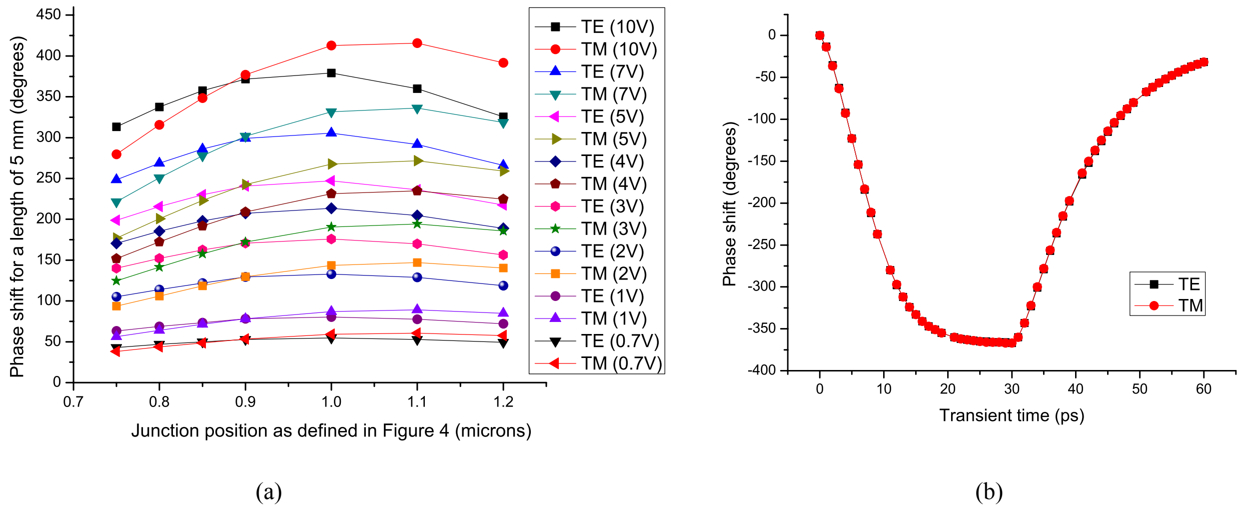
Figure 5(a) shows the resulting phase shift achieved for different junction depths and applied voltages. For the V-groove junction device, polarization independence during modulation is achieved when the top of the V-groove junction is situated around 0.87 μm with respect to the bottom of the waveguide. The flat junction modulator achieves polarization independence with a junction situated at approximately 0.5 μm from the bottom of the waveguide [27]. For a waveguide length of 5 mm, the V-groove modulator achieves a phase shift of 365° ($L_\pi V_\pi$ =2.5 V-cm) for an applied reverse-bias voltage of 10 V. However the flat junction device only obtained a maximum phase shift 290° (($L_\pi V_\pi$ = 3.1 V-cm) for the same applied voltage. These results demonstrate that the V-groove p-n junction device can achieve the same efficiency as the modulator proposed in [Fred] without the issues involved with submicron waveguides.

The next step is to determine the bandwidth of both modulators. This is done by calculating the phase shift against the transient time. The result of the V-groove device is shown in Figure 5(b) for TE and TM polarizations. The transient response times were found to be similar for both types of junction. The V-groove device has a rise time of 13 ps and a fall time of 23 ps for both polarization states. For the flat junction device, the rise time is 12 ps and the fall time is 21 ps for both polarization states [27]. These results correspond to an intrinsic bandwidth in excess of 15GHz for a relatively large-area waveguide modulator.

3.2. High-speed Switches

We are currently developing an SOI optical switch that utilizes the physical effect of Total Internal Reflection (TIR). Similar to the modulator discussed above, the switch works by generating free carriers at the junction of crossing waveguide structure (see Figure 6). The carriers induce a refractive index change that is lower than the intrinsic index of

silicon. Light traveling along the input waveguide is reflected from this region of lower index into the output of the crossing waveguide. If no charge is present, the light continues to propagate along the original waveguide to its output. Several TIR-based switches have been reported in the literature where attempts have been made to confine or guide injected carriers to the crossing region [31-33]. However these configurations have lacked the ability to stop the diffusion of carriers from their desired position into the rest of the device. This results in reduced efficiency of the device. These 'stray' carriers may also cause unnecessary optical loss in other regions of the switch. Several device modifications have been made to overcome this and several other issues.



(a) (b)

Figure 5. (a) Determination of the polarization independent phase shift as a function of the depth of the p-n junction in the waveguide. (b) The modeled time-dependent response of the V-groove modulator.

In order to make more efficient use of the injected carriers, a barrier region has been introduced into the intersection region of the two waveguides, as shown in Figure 6. This barrier is created by etching away a region of the intersection area, growing a thin insulating oxide layer, and then back-filling the etched region with polysilicon. Current injected into the active region is therefore confined by the insulating oxide layer thus creating a more efficient use of the concentrated carriers.

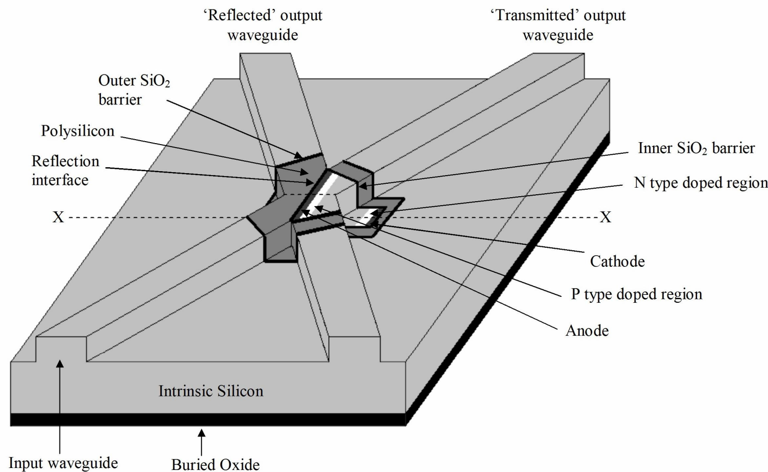
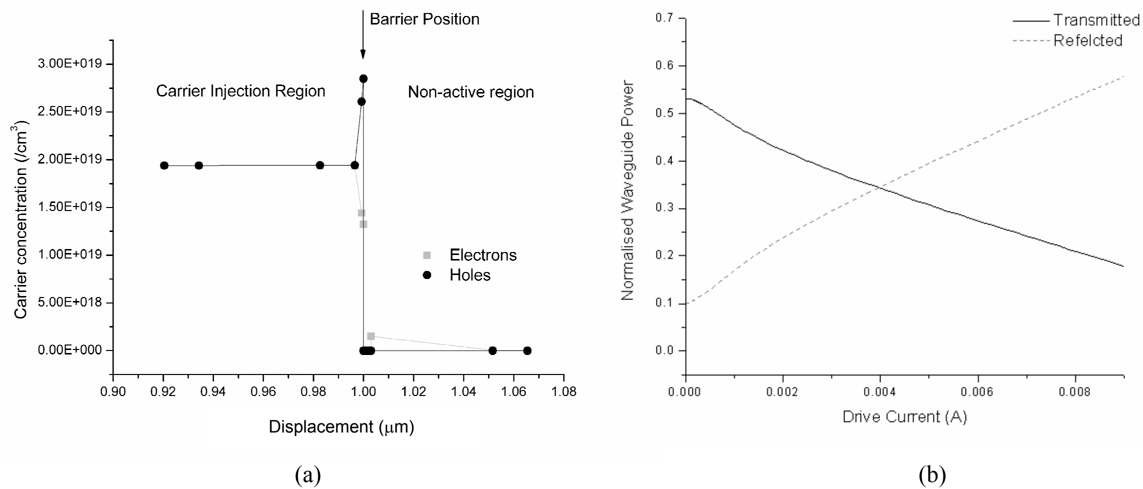


Figure 6. Schematic of an enhanced TIR crossing waveguide switch [34].

Shown in Figure 6, the oxide barrier inside the waveguide crossing region is positioned so as to create a precise reflection interface. Away from the reflection interface the barrier is designed to cross the waveguides perpendicular to the direction of the optical mode propagation in order to minimize any perturbation of the propagating light. The use of such a barrier in silicon photonic devices has been demonstrated in recent years to form a MOS phase modulator and in other phase shifting based devices without significant perturbation of the optical mode [24].

Electrical simulation of the switch was carried out using Atlas to demonstrate the ability of a thin SiO_2 barrier to minimize the diffusion of carriers. The modeled structure consisted of a non-active silicon region (the area outside the charge injection region) separated by a 3 nm SiO_2 vertical barrier from an active silicon region (representing the charge injection region). The carrier concentration along a line perpendicular to the barrier was examined for an applied forward bias. This carrier concentration has been plotted in Figure 7(a) with the position of the barrier located at 1μm. The modeling suggests there is negligible diffusion across the oxide barrier. It can therefore be assumed that the active region of the device is well isolated.

Electrical simulations for both carrier concentration as a function of drive current and the transient response for a device with rib height 4μm, rib width 2.8 μm, slab height 1.77μm was also carried out [34]. From these simulations, the index change as a function of drive current can be determined by using the equations of Soref and Bennett [35]. The resulting reflection due to TIR can be determined as a function of drive current. This result is shown in Figure 7(b) for TE polarized light. A drive current of approximately 8 mA is required to switch the output power from the transmitted output waveguide to the reflected output waveguide. It should be noted that the optical power in the reflected arm for no applied current is due to crosstalk. An improvement in crosstalk through the use of tapers is discussed in [34] for use in future device modeling. The transient response of these devices has also been modeled. The response time of the proposed switch configuration is approximately 2 ns [34]. This corresponds to a bandwidth in excess of 100 MHz.



(a) (b)

Figure 7. (a) The effect of the vertical oxide barrier on carrier concentration in the device. (b) The effect of switching as a function of applied drive current.

4. RING RESONATORS

The versatility of small ring resonators makes them well suited as wavelength selective devices for integrated optical circuits [36]. Since the Free Spectral Range (FSR) is inversely proportional to the resonator circumference [17], this implies that the resonator radius needs to be 5 μm or less if an FSR of 30nm or more is to be achieved. The strong

confinement capabilities of strip waveguides are most likely necessary to minimize the loss at these sorts of radii. This then implies that submicron cross-sectional dimensions are necessary to allow for single-mode operation of the resonator. However submicron waveguides require fabrication processes with strict tolerances, are prone to issues with sidewall roughness and are difficult to make polarization independent [9].

One potential solution to these issues is to use larger waveguide cross-sections in conjunction with multi-stage, parallel- or serial-coupled ring configurations. This solution would allow two rings of slightly different circumference (and resonance conditions) to resonate only when the resonance conditions of both rings is met. The resonant condition that has to be satisfied is given by:

$$FSR_{net} = m \times FSR_1 = n \times FSR_2, \quad (1)$$

where m and n are integers, FSR_1 and FSR_2 are free spectral ranges of the two resonators, and FSR_{net} is the net free spectral range of the two-level series coupled resonator.

Modeling has demonstrated that ring resonators with relatively large circumferences comprised of rib waveguides can obtain significant improvement by adding multi-stage rings. For example, by multiplying the experimental responses for resonators with radii of 25 μm and 50 μm a predicted net FSR of approximately 2 nm can be obtained, as shown in Figure 8. The experimental result of the drop port of a cascaded ring resonator device is shown in figure 9. This particular device has ring radii of 50 μm and 100 μm.

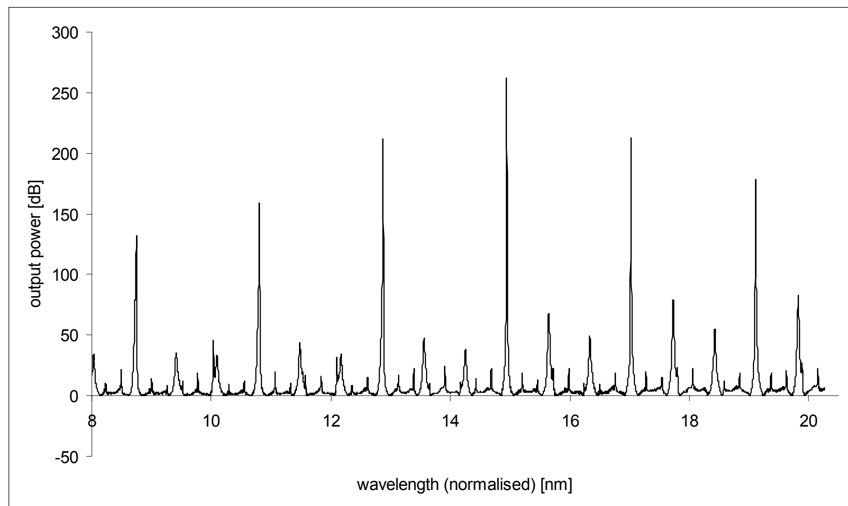


Figure 8. Modeled spectral response of a cascaded rib waveguide ring resonator consisting of one ring with a radius of 25μm and a second ring of 50 μm.

It should be noted that this method of improving the FSR does have a drawback in that if the quality of the rings is poor and/or equation 1 is not strictly met, rather prominent side lobes may appear in the spectra as can been observed in Figure 9. This issue may be solved by improving the fabrication quality of the resonators as well as modeling the resonators in greater detail to determine the critical parameters more accurately. Nonetheless this method may have significant benefits over using resonators comprising strip waveguides as lithography tools with less resolution can be utilized, it is easier to contact to larger waveguides as would be the case for active devices, and it is easier to determine a polarization independent resonator.

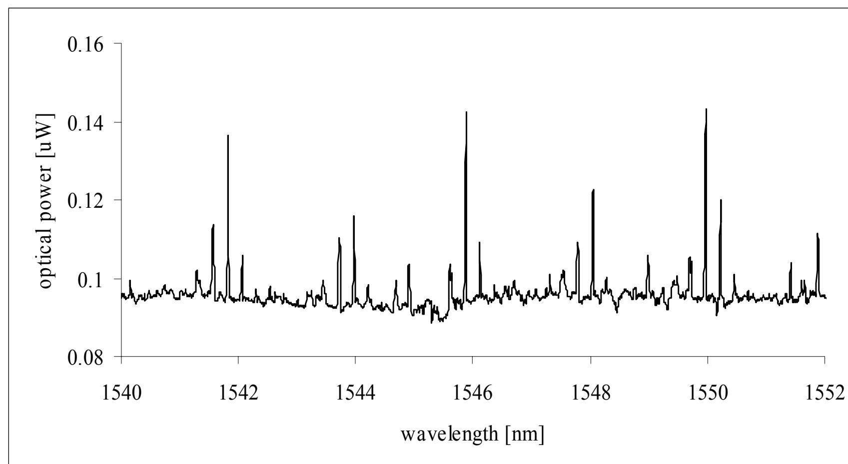


Figure 9.The drop port spectral response of an experimentally measured cascaded ring resonator device

5. PROTON BEAM WRITING

While much of the work done at Surrey is done in the SOI material system, we are also actively investigating waveguide fabricated on regular silicon substrates. These waveguides would be more suitable for longer wavelength applications (except in the 3–3.5 µm range) due to the absorption of the buried oxide layer at these wavelengths [9]. Silicon-based long wave infrared photonics could find applications in several areas including sensing, communications, signal processing, missile detection and imaging. In order to fabricate waveguides on a standard silicon substrate a method of Proton Beam Writing (PBW) is being studied. PBW is an advanced lithographic technique for developing semiconducting substrates on the submicron scale. Typically it utilizes a high-energy ion microbeam to irradiate suitable resists (e.g. SU-8 & PMMA). Subsequent wet etching is then employed to develop the resist. While it was initially investigated for producing latent microstructures in high molecular weight PMMA resist, several authors have demonstrated PBW as a method to direct write three dimensional structures directly in silicon thereby eliminating the need for a photoresist [37].

PBW works by irradiating the silicon crystal structure with a high-energy, well-focused proton beam. By increasing the doping density, the defects at the surface of the proton irradiated region create a current barrier. During electrochemical etching, the current density at the surface of the proton irradiated region is much lower than the non-irradiated silicon. As the etch progresses, the etch will continue to remove the non-irradiated silicon as it has a lower resistance path for the current [38]. PBW has already demonstrated its potential as a next generation lithography technique in silicon-based applications. Free standing bridges, multilevel structures, and high aspect-ratio nano-tips fabricated in silicon have been demonstrated [37, 39].

PBW has several key advantages over conventional photolithography. It is a direct write process it eliminates the need for a potentially costly mask. Furthermore, when prototyping new devices that may require small structural modifications, subsequent devices can be produced simply by modifying the scan of the microbeam. This is an attractive benefit from a cost point of view as modifications using conventional lithography require the layout and production of an additional mask. Also, the position, depth, and amount of damage can also be controlled by controlling the proton beam's energy, fluence, and beam scan rate. The result is that three dimensional structures can be realized using this method.

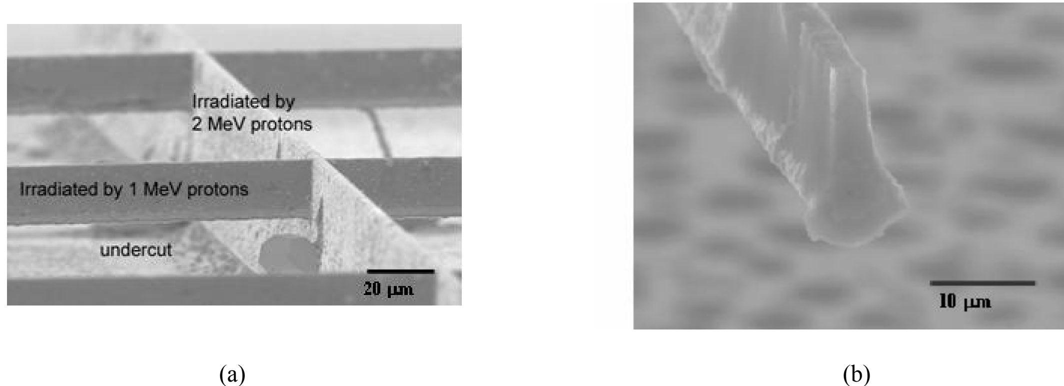
In order to fabricate free standing waveguides, two different ion energies are required. A high energy implant is used to create pillars upon which the waveguides are supported. A lower energy implant is subsequently used to create the waveguides. Based upon the simulation results obtained by SUSPRE, 2 MeV protons travel approximately 50µm into silicon, and 1MeV protons penetrate approximately 17 µm. The pillars were therefore created by irradiating the silicon with a dose of 0.7×10^{15} protons/cm^2 at an energy of 2 MeV and the waveguides with a dose of 0.6×10^{15} protons/cm^2 at

an energy of 1 MeV. Two scans of the microbeam were made over the same position in order to create the localized damage pattern. The doses are significant enough to inhibit the current flow in the irradiated regions, thereby limiting the formation process of porous silicon during electrochemical etching. The details of the electrochemical etch can be found in .

A Scanning Electron Micrograph (SEM) showing the waveguides and support pillars is shown in Figure 10(a). A SEM of the free-standing waveguide facet is shown in Figure 10(b). The waveguide has a 'tear-drop' shape with a height of 17μm, and width of 3.7 μm at the top and 8 μm at the bottom. This shape is likely due to the lateral spreading of the beam with depth, but it can likely be altered in the future by alternative choices of irradiation energies.

Propagation loss measurements were performed at the wavelength of 1550 nm in order to compare it with the loss of standard (SOI) silicon waveguides prevalent in the literature. The free-space experimental test setup is identical to the one used in [17]. The propagation loss was determined using the cut-back method [28]. In order to polish back the waveguides, they were first potted in a transparent wax. The wax prevented the waveguides from moving and hence from being damaged during polishing. The propagation loss was determined to be 13.4±0.7 dB/cm for TE and 14.6±0.6 dB/cm for TM polarized light respectively.

It is believed that there are two main reasons for the high propagation losses obtained. The first is that the sidewall roughness of the waveguide as well as irradiation damage of the waveguide itself during the PBW. It is expected that the irradiation damage could be reduced by modification of the fabrication process to include an annealing step. Oxidizing the waveguides may also help to alleviate the roughness. While the propagation loss values reported here are rather high, they are nonetheless promising especially when compared to the propagation loss of ~ 25 dB/cm that was measured for early SOI waveguides (e.g. reference [40]). Therefore, it can be expected that further improvements of the fabrication process will result in much lower propagation loss of the free standing waveguides, increasing the viability of this technology for mid and far IR photonic applications.



(a) (b)

Figure 10. (a) SEM micrograph of the resultant free-standing waveguides as a result of PBW. (b) The end-facet of a waveguide.

6. CONCLUSIONS

Herein we have discussed some of the main areas of Silicon Photonics that the University of Surrey is engaged in. We have made efforts to improve upon the issue of coupling fibers to and from photonic chips using DGADC's whose theoretical coupling efficiency can reach approximately 90%. Work has also begun in attempting to realize the potential of ion beam implantation to create grating structures. We have demonstrated that by employing rib waveguides of the order of 1μm in cross sectional dimension, optical modulators can still be very fast (bandwidth ~15GHz), but may also exhibit polarization independent performance. We have also demonstrated the means to fabricate high-speed, highly-efficient switches. Ring resonators based upon micron-sized waveguides can be made to have larger FSR's by utilizing multi-ring configurations are also feasible. Finally, we have demonstrated that advanced fabrication techniques may be possible to realize silicon waveguides fabricated in standard silicon wafers for long wavelength applications.

The field of Silicon Photonics is continuing to grow and there is no indication of it slowing in the near future. While significant breakthroughs have been made in the field, there are still many areas for improvement and study. While we have attempted to outline some of the key areas of our research we believe that there are still many more exciting and significant benefits to be obtained from the field of Silicon Photonics.

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