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Oxidation smoothening of silicon machined micro- and nano-scale structures

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ABSTRACT

We have developed a process to machine bulk silicon in two- and three-dimensions shapes and structures. Here we briefly introduce this process and give examples of the types of surface profiles and three-dimensional geometries which can be fabricated. One of the limitations, as with all forms of silicon machining is the final surface roughness, as this introduces losses, for example in light propagation through photonic devices. Here we describe various contributing factors to the surface roughness and options to reducing it. Under optimized conditions roughness values of less than 1 nm can be achieved.

1. Introduction

Recent developments in micro- and nano-fabrication technologies have opened up opportunities in diverse fields and contributed to a new phase for developments of miniaturized devices. Although a variety of different materials can be used, silicon is the material of choice because of the availability of wide range of manufacturing facilities, mostly developed for integrated circuit fabrication. It is also a semiconductor with unique mechanical and optical properties [1]. A technique capable of fabricating complex geometries of silicon structures and shapes can contribute significantly to the development of the new generation of micro- and nano-devices.

We recently developed a process for micro- and nano-machining of a variety of structures and components in silicon using a combination of ion irradiation and electrochemical anodization. Different types of silicon surface patterns, three-dimensional wires, complex free-standing structures, etc., were fabricated [2,3]. For many applications, controlling and/or reducing the surface roughness [4–6] is a key factor, such as holographic silicon surfaces [7], low loss silicon photonic components [8], micro/nanoelectromechanical systems [9–11], high q-factor nanoresonators [10,12] and microcavities [13,14]. For commercially available silicon wafers, the surface roughness is usually less than 0.2 nm. Any fabrication process is therefore likely to degrade this extremely smooth surface.

The specular reflection, R_s, of a wavelength λ, from the root mean square surface of roughness σ of a perfect conductor at normal incidence is:

$$R_s = R_o \exp[-(4\pi\sigma)^2/\lambda^2] \quad (1)$$

where R_o is the reflection from a perfectly smooth surface of the same material [15]; clearly a low roughness is desirable to achieve a high reflectivity. For infrared light scattered by the surface roughness of silicon waveguides, a number of studies have been conducted [8,16,17]. In [16] it was found that the measured propagation loss through a waveguide fabricated with a typical sidewall roughness of 9 nm reduced to a minimum value of 0.1 dB/cm when the roughness was reduced by oxidation to 0.5 nm. In another example [8] oxidation reduced the propagation loss through waveguides fabricated using our process from 3 dB/cm to ~1 dB/cm, with the surface roughness being reduced from ~17 nm to 3 nm. One puzzling aspect of our prior work was the large surface roughness values measured directly after fabrication and how rapidly these were reduced by the effects of thermal oxidation. Therefore, it is important to better study surface roughness of silicon components fabricated using our machining technique and find means of minimizing this, to enhance its potential for fabricating different

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arbitrary-shaped smooth silicon micro- and nano-structures [2,18]. Here we describe examples which highlight the dual effect of oxidation in not only reducing the roughness of the silicon surface, but also, and just as importantly, remove all residual traces of low porosity silicon from the anodized surfaces.

Our machining process uses high-energy ion irradiation, typically 100–2 MeV protons and helium ions, of p-type silicon wafers, followed by electrochemical anodization in a hydrofluoric acid (HF) solution. Anodization of silicon forms porous silicon (PSi) where the surface is partially dissolved away, leaving a sponge-like network in which nanocrystalline silicon islands remain [19,20]. Ion irradiation of silicon causes crystalline damage (Fig. 1(a)), mainly as vacancy-interstitial pairs. These act as trap levels where charge carriers undergo recombination, reducing the hole density and increasing the resistivity along the ion trajectories [21]. Ion irradiation thus alters the hole current flow during subsequent electrochemical anodization, allowing the anodization rate to be slowed/stopped for low/high fluences. For moderate fluences the anodization rate is selectively stopped only at depths corresponding to the high defect density at the end-of-range, giving a machining technique for true 3D silicon micro/nano-fabrication. The underlying silicon structures which are buried in a PSi layer may be easily revealed by removing the PSi with dilute potassium hydroxide (KOH). This 3D silicon micro and nanomachining process has the potential to provide a wealth of new types of structure for silicon photonics, M/NEMS and BioMEMS.

2. Precisely controlled 3D silicon and PSi surface patterning

This machining approach can be used for fabricating precisely-controlled 3D silicon and PSi surface patterns. At a low fluence irradiated line, PSi is formed at the surface, and only close to the ion end-of-range does the defect density become high enough to allow the formation of a narrow tip at the top of the end-of-range core, Fig. 1(b). So if the anodization is stopped just when the tip of the core is exposed, a sharp region forms, Fig. 1(c). In comparison, in wider, heavily-irradiated regions, anodization is totally stopped, while PSi forms on either side, producing a tall, wide silicon region. Fig. 1(c) shows the resultant shapes of the low-fluence, narrow

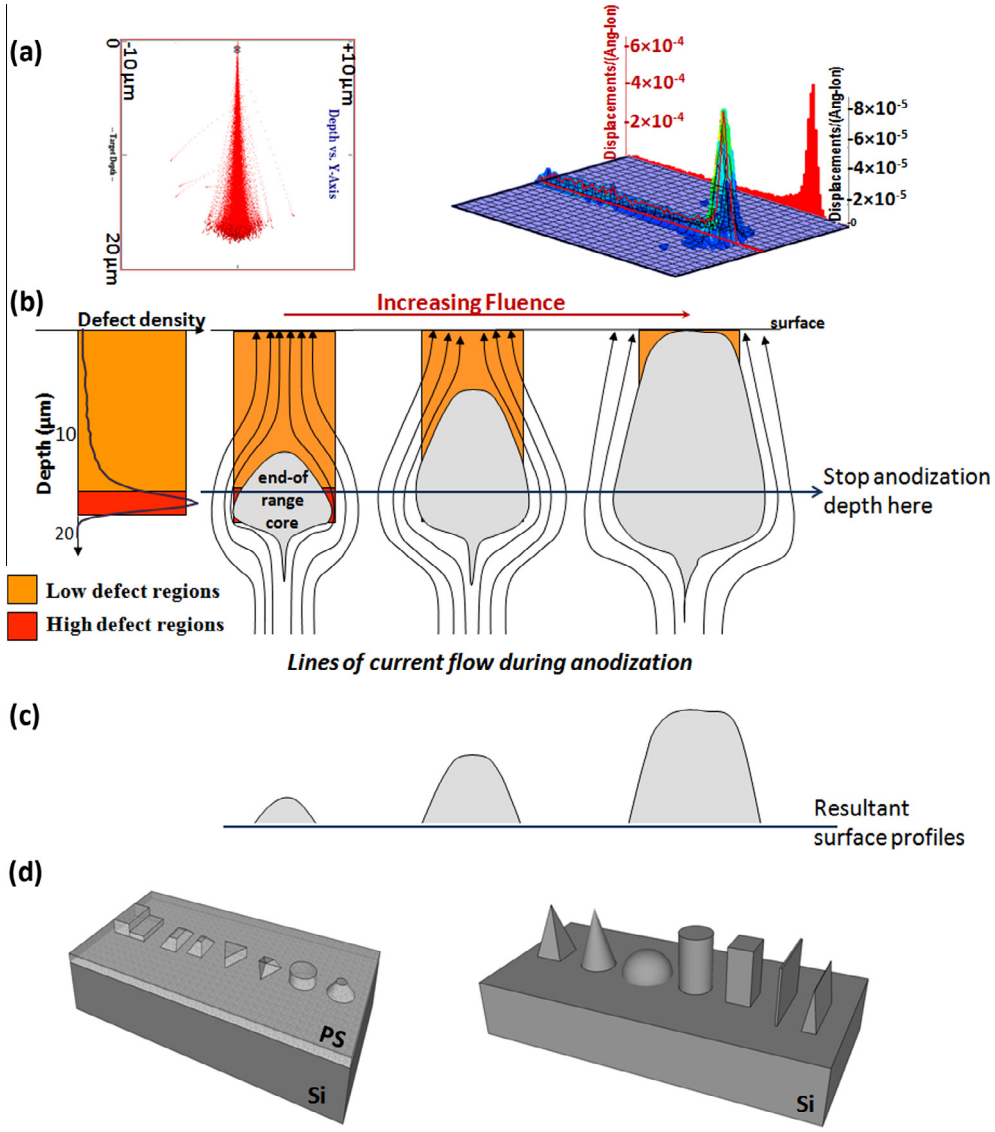

Fig. 1. (a) SRIM simulated trajectory and defect density plot versus depth for 1 MeV protons in silicon [27]. (b) Schematic of the damage profile and deflected hole current around high defect region during anodization. (c) Schematic of electrochemical anodization process in which the end-of-range region remains as solid silicon. (d) Basic shapes that can be machined on PSi and silicon surfaces.

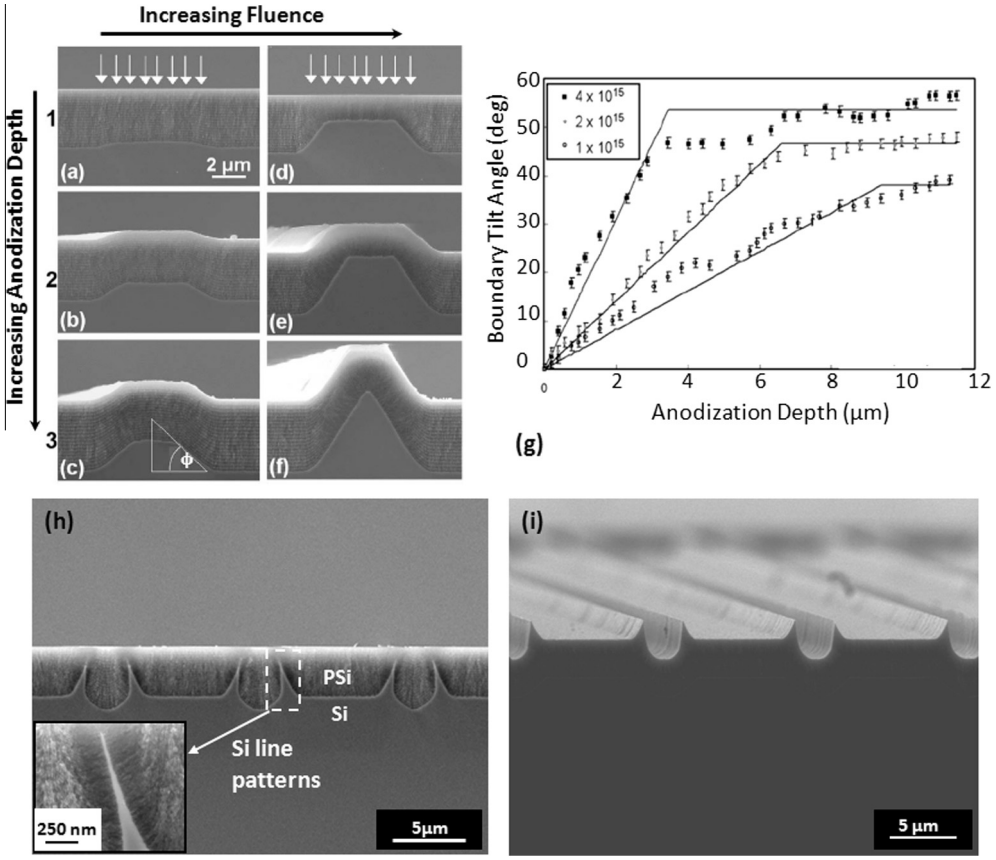

Fig. 2. Cross-sectional SEMs of silicon lines forms by irradiating 6 μm wide line, 2 mm in length with fluence of [(a)–(c)] $2 \times 10^{15}/cm^2$ and [(d)–(f)] $4 \times 10^{15}/cm^2$. (g) Plot of φ versus anodization depth for different fluences [22]. (h)–(i) Cross-sectional SEMs showing silicon lines with sharp nanometer tips (h) before (i) after removal the PSi.

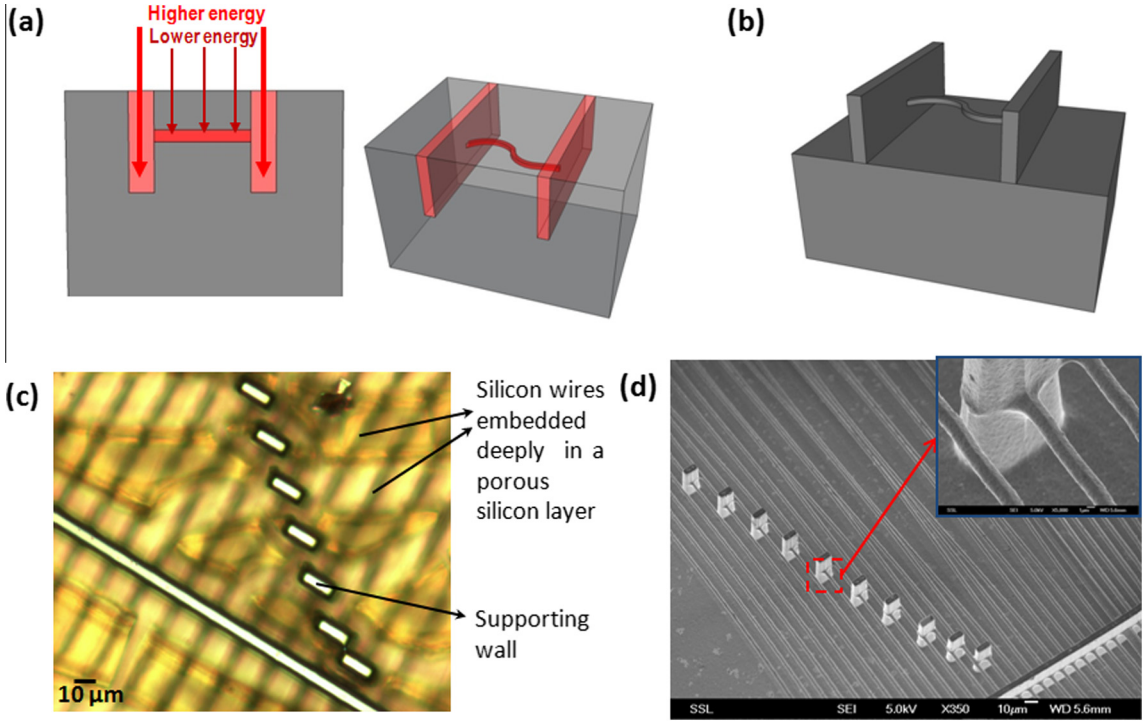

Fig. 3. Schematic showing the fabrication of suspended 3D wires using (a) low fluence irradiation to form the wire and high fluence, higher energy irradiation to form the supporting walls, (b) anodization and removal of PSi. (c) Deep silicon wires in PSi and (d) completely suspended silicon wires after PSi removal.

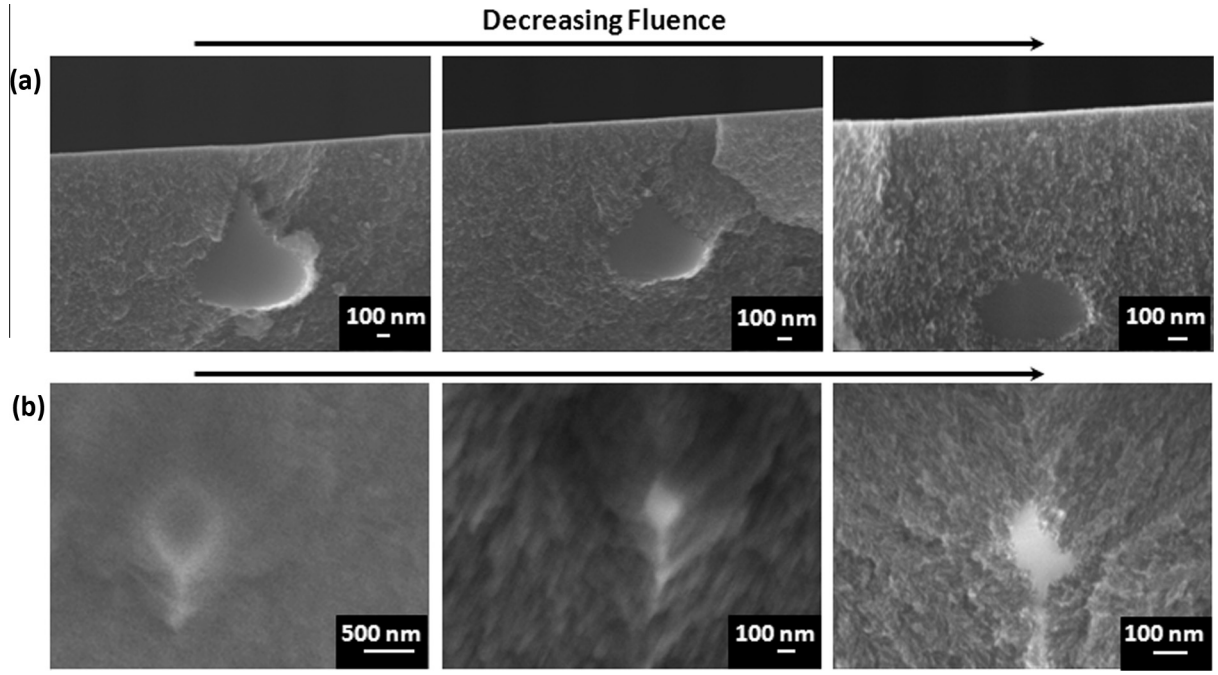

Fig. 4. SEM cross-section images of silicon nanowires fabricated with 200 keV protons in (a) 0.02 Ω cm wafer with line fluences of 1×10^{11}, 4×10^{10} and 2×10^{10}/cm and (b) 0.1 Ω cm wafer with 3×10^{10}, 1×10^{10} and 8×10^{9}/cm, respectively.

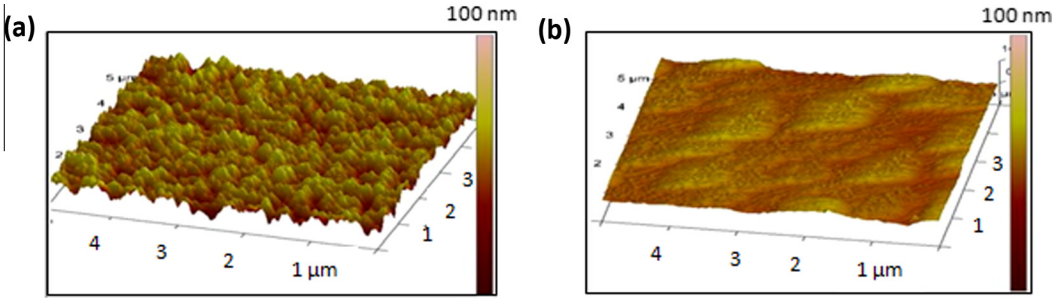

Fig. 5. AFM images of a silicon surface (a) after fabrication, (b) after megasonic cleaning.

region, and high-fluence, wide region where anodization is stopped above the end-of-range depth.

Controlling the irradiation and electrochemical anodization conditions gives flexibility in fabricating complex surface patterns. Fig. 1(d) shows schematics of 3D silicon and PSi surface patterns which can be patterned using our process. At a fixed irradiation energy, the most important factors influencing the shape and dimensions of the surface patterns are fluence and anodization depth. Fig. 2(a)–(f) show the effect of these factors for wide areas irradiated using proton beam writing (PBW) with 2 MeV protons [22]. The range of 2 MeV protons in silicon is ~50 µm, with a uniform rate of defect production for the first 40 µm of penetration, hence ideal for studying the evolution of the irradiated shape versus anodization depth and fluence within a region of uniform defect density. Fig. 2(a)–(c) and (d)–(f) show the effect of anodization depth for two different 6 µm wide line areas irradiated with 2 MeV protons with a fluence of 2×10^{15}/cm^2 and 4×10^{15}/cm^2. As a result of the dependence of etching rate on fluence, there is a boundary between the irradiated and unirradiated portions which becomes progressively more tilted with etch depth and with increasing fluence. Fig. 2(g) shows the measured boundary tilt angle φ versus anodization depth for different fluences; φ increases approximately linearly with depth until it reaches a constant value. For increasing fluence, φ increases at a particular etch depth. Under conditions of a high fluence, shallow anodization depth and wide irradiated area, an anodized surface with a flat top is generally observed, whereas for a low fluence, deeper anodization depth or narrow irradiated area a triangular shape is more likely to be observed as all these conditions favour the anodization fronts from either side meeting in the middle of the irradiated region. The PSi can be removed, revealing the 3D surface patterns. 3D PSi surface patterns can also be produced by removing the PSi after partially anodizing the sample and repeating the anodization step to form a PSi surface profile of the revealed silicon [22].

Fig. 2(h) and (i) show another example of silicon surface patterning using the large area irradiation facility at CIBA to irradiate a wafer covered with a line/spacing patterned photoresist. The sample is irradiated with 450 keV protons and a fluence of 1×10^{15}/cm^2 to produce silicon lines with very fine tips. The photoresist has flat top with a thickness sufficient to stop the ions, however its thickness is gradually varying at edges, modifying the end-of-range defect depth profile of ions in the silicon wafer beneath. Fig. 2(h) shows the wafer after anodization and Fig. 2(i) shows the sample after removing the PSi layer to reveal the silicon surface pattern beneath having arrays of lines with very sharp nanometer tips.

These precisely controlled silicon and PSi surface patterns are useful in fields such as photonics, M/NEMS, BioMEMS and

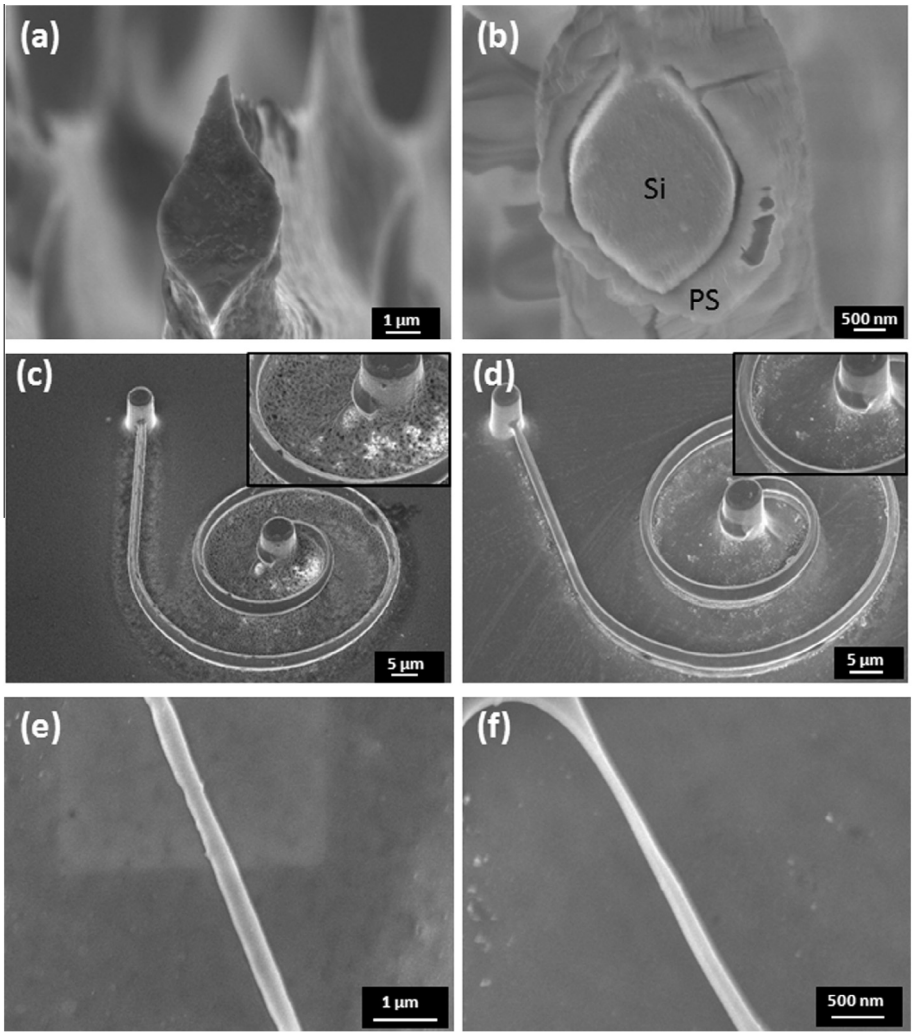

Fig. 6. SEMs showing (a) silicon wire before (b) after oxidation. Suspended silicon spring (c) before and (d) after oxidation and immersion in HF. The inserts show the effectiveness of oxidation in removing the remained PSi, leaving behind a smooth silicon surface. (e) and (f) Machined smooth silicon nanowires after oxidation.

microfluidics. Alternatively, they can be used as a master copy for imprint and transfer the pattern to another substrate [23,24].

3. 3D suspended silicon micro and nano-machining

Fabrication of true 3D micro- and nano-patterned components of silicon-based materials are of great interest for many fields, enabling the fabrication of 3D integrated systems which can improve device performance and packing density. Our process allows this, as well as the ability of fabricating custom-shape structures. For high-energy protons in silicon the localized defect density at the end-of-range is significantly higher than along their penetration path [3], Fig. 1(a), our process utilizes this to fabricate 3D micro and nanostructures in bulk silicon.

We have fabricated a variety of complex, arbitrary shapes, curved or multilevel silicon wires and structures [2,3,25,26]. By controlling moderate fluences delivered to points within an irradiated area, the resistivity at the end-of-range, can be locally increased [21], Fig. 3(a). During subsequent anodization the flow of electrical holes from the back surface bends around the high defect regions to the front surface. By etching beyond the ion end-of-range, PSi forms around these highly defective regions, leaving the core region intact, with a size and depth mainly depending on the proton fluence and energy. The PSi can then be removed for revealing the 3D suspended silicon structures, Fig. 3(b).

We have fabricated arrays of long, suspended micro and nanowires from bulk silicon wafer, using PBW due to its great flexibility in delivering different fluences to different locations. High energy proton irradiation at high fluence was used for fabricating the supporting walls for the suspended wires by completely stop the anodization in these irradiated regions. Fig. 3(c) shows a plan-view optical image of silicon wires embedded in PSi after anodization. Diluted KOH solution can be used for removing the PSi and making the wires completely suspended, Fig. 3(d).

The 3D suspended silicon wires can have different shapes and different cross-sectional profiles over dimensions from tens of microns to tens of nanometers. The most important factors influencing the core shape and size are the ion energy, irradiation fluence and irradiated surface width. For studying the range of cross-section profiles of the wires, we present micron-size wires which are easy to image and study the evolution of their shapes. This is important in defining how best to fabricate suspended wires with this micromachining approach for different applications. Irradiation of broad line widths can be done through scanning several adjacent lines using PBW or using a surface mask with wide micron-size openings followed by large area irradiation.

While high energy proton irradiation allows deeper penetration into the silicon, forming a core further beneath the surface of the

wafer, the ions are more scattered [27], so defects are distributed further away from the beam axis and larger core sizes are typically produced. This should be considered when the fabrication of small size cores of tens or few hundreds of nanometers is desired. Fig. 4 shows example of nanowires fabricated using a lower proton energy of 200 keV, showing how the core size varies with fluence in two different wafer resistivities. Using even lower proton energies and fluences smaller dimension nanowires can be fabricated [25].

4. Smoothening the 3D silicon micro and nanomachined structures

For many applications it is important to fabricate structures which are very smooth [8–12]. After fabrication, small particles of silicon or porous usually remain on the surface (Fig. 5(a)). A variety of processes can be used for cleaning and reducing the silicon surface roughness, e.g. megasonic cleaning is effective at removing remaining silicon particles, Fig. 5(b). Another procedure for reduction of the surface roughness, as well as removing the remaining particles on the surface, is thermal oxidation of the wafer in air or flowing oxygen [16,17] and subsequent removal of silicon oxide by dilute HF. Applying a large electropolishing pulse after anodization is another approach of smoothing the surface and separating the PSi layer [21,28,29]. However, depending on the application, some of these processes may not be appropriate. For instance, megasonic cleaning and electropolishing are not suitable for reducing the roughness of a delicate, 3D nanopatterned surfaces and suspended nanostructures. Thermal oxidation is the most useful approach for roughness reduction of these 3D silicon structures after fabrication and also for cleaning the remaining PSi particles. It can also reduce the structure dimensions and hence fabricate smooth, 3D silicon nano-scale components. Fig. 6(a) and (b) show a cross-section of a suspended wire before and after thermal oxidation. The oxidized layer can be removed by immersion in dilute HF.

Fig. 6(c) and (d) show another example of thermal oxidation on smoothening and reducing the size of a micromachined, suspended silicon structure. Fig. 6(c) shows a spring held in place by high-fluence irradiated pillars after irradiation, anodization and immersion in KOH. However, the PSi is not completely removed, causing high surface roughness and residues on the surface. Subsequent thermal oxidation is very effective in cleaning the sample by converting the PSi to oxidized PSi as well as reducing the underlying silicon surface roughness by oxidation of the silicon core. These layers can be removed, leaving smooth suspended 3D silicon spring and surfaces, Fig. 6(d).

Starting from wider wires, followed by thermal oxidation and removing the oxide layer, smooth silicon nanowires with diameter of less than 100 nm can be fabricated, Fig. 6(e) and (f). By repeating the oxidation process the wire diameter shrinks, enabling smooth, suspended 3D silicon nanostructures with diameter of few tens of nanometer to be fabricated.

5. Conclusion

We have developed a micromachining process to fabricate a range of micro- and nano-scale components and structures. Typical measured surface roughness values for as-fabricated structures can be large, up to 20 nm, but this is misleading as it is largely due to the presence of a low porosity layer clinging to the anodized surfaces. This can be remedied by thermal oxidation which removes the oxidized PSi and smoothens the underlying silicon surface, depending on the oxidation temperature and duration.

Acknowledgments

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