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# Nanoscale lithography of $LaAlO_3/SrTiO_3$ wires using silicon stencil masks

**S Azimi[1,2], J Song[1], C J Li[3,4], S Mathew[3,5], M B H Breese[1,2,3] and T Venkatesan[3,4,5]**

[1] Centre for Ion Beam Applications (CIBA), Department of Physics, National University of Singapore, Singapore 11754222
[2] Singapore Synchrotron Light Source (SSLS), National University of Singapore, 5 Research Link, Singapore 117603
[3] NUSNNI-Nanocore, National University of Singapore, Singapore 117411
[4] National University of Singapore Graduate School for Integrative Sciences and Engineering (NGS), National University of Singapore, 117456 Singapore
[5] Department of Electrical and Computer Engineering, National University of Singapore, Singapore 117576

E-mail: phymbhb@nus.edu.sg

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**Abstract**

We have developed a process to fabricate low-stress, fully crystalline silicon nanostencils, based on ion irradiation and the electrochemical anodization of p-type silicon. These nanostencils can be patterned with arbitrary feature shapes with openings hundreds of micrometers wide connected to long channels of less than 100 nm in width. These nanostencils have been used to deposit (2.5 $\mu$m- to 150 nm-wide) lines of $LaAlO_3$ (LAO) on a $SrTiO_3$ (STO) substrate, forming a confined electron layer at the interface arising from oxygen vacancies on the STO surface. Electrical characterization of the transport properties of the resulting LAO/STO nanowires exhibited a large electric field effect through back-gating using the STO as the dielectric, demonstrating electron confinement. Stencil lithography incorporating multiple feature sizes in a single mask shows great potential for future development of oxide electronics.

Keywords: nanostencil lithography, conducting nanochannels, LAO/STO patterning, transport properties, 2D electron gas, silicon micromachining

(Some figures may appear in colour only in the online journal)

$LaAlO_3/SrTiO_3$ (LAO/STO) interface conductivity [1] has attracted enormous interest, due to both the physical properties [2–4] and nanostructured applications of this system [5–9]. Notable examples include a biased atomic force microscopy (AFM) tip-induced metal-insulator transition of LAO/STO [10], which can be used to write and erase conducting patterns on an initially insulating sample. With this technique, a single electron transistor [11, 12] and a photodetector [13] based on LAO/STO have been demonstrated; it was found that ~10 nm-wide LAO/STO conducting wires have anomalously high mobility [14] at room temperature. This AFM technique is ideal for creating precise nanostructures, but the limited patterning speed is obvious. On the other hand, photolithographic postpatterning of LAO on STO has achieved conducting wires with widths of about 10 $\mu$m [15, 16]. Between these two extremes, wires with widths ranging from a micrometer to a few nanometers have been less studied, though devices based on this length scale would probably be the starting point for oxide-based nanoelectronics. In this paper, we describe a new type of silicon nanostencil for lithography that fabricates various LAO/STO nanostructures with feature widths that range from hundreds of micrometers to hundreds of nanometers, and we explore their transport properties.

Although many nanoscale patterning techniques have been developed in recent years [17–20], stencil lithography is attractive in providing a single-step, rapid process which is capable of achieving multiscale patterns over large areas [21–27]. Another attractive feature is that a patterned resist stage is not required, so unconventional, biosensitive, or fragile

 

surfaces, or even three-dimensional (3D) surfaces, can be patterned using a reusable stencil mask. Nanostencil lithography has been used to pattern various large arrays of nanoscale features such as dots [22] and wires [23–25], with resolutions down to 50 nm and metallic structures on polymer substrates [26]. Nanostencil lithography has been used for high-throughput fabrication of infrared plasmonic sensors [28], to create arrays of molecular patterns with a spacing of less than 400 nm and features down to 50 nm [29], and to fabricate aluminum and gold nanowires less than 100 nm wide and several micrometers in length [24]. The stencil membrane is typically made of low-stress silicon nitride with a thickness of 100 nm to 1 $\mu$m, depending on the required minimum feature size. High-resolution openings are patterned using electron beam (e-beam) lithography or a focused ion beam (FIB). The masks should contain as little stress as possible in order to avoid catastrophic failure of the mask, either during fabrication or during pattern transfer where the deposited layers can cause membrane deformation. Efforts to create stabilized structures include corrugations or supports from large, adjacent silicon support frames [30–32].

A different approach to fabricating large-area, low-cost stencil masks was developed [33] based on photolithography and anisotropic etching of microscale and nanoscale openings in a suspended crystalline silicon membrane. This allows a more robust structure than a silicon nitride membrane of similar thickness, and allows openings to be defined with anisotropic wet etching, which is a rapid, wafer-scale patterning process. However, the shape of the patterns is limited by the anisotropic etching dependence on the directions and angles within the crystalline silicon. In [34], a crystalline silicon membrane was fabricated using standard techniques combined with FIB to create 150 nm-wide openings, about 3 $\mu$m long, spanning a 5 $\mu$m-wide gap. The membrane thickness of 1–10 $\mu$m after the initial silicon etch was fine-tuned using reactive-ion etching (RIE) to reduce the overall thickness to less than 2 $\mu$m. Stiffening structures were integrated into the membranes in an attempt to overcome the problem of membrane bending. This process requires multiple fabrication and deposition steps and extensive FIB machining, with its associated limitations in device throughput and fabrication time.

We have developed a nanostencil mask fabrication process to make low-stress, fully crystalline silicon membranes using a patterning process based on ion beam irradiation and electrochemical etching, which enables arbitrary shape patterns in different membrane thicknesses to be easily combined and mass produced. Such integrated patterning of openings from greater than 100 $\mu$m to less than 100 nm in width allows deposition of narrow conducting channels, which are connected to large-area contact pads, to be patterned in a single step. We describe the nanostencil fabrication process and its ability to deposit patterned LAO nanowires on STO substrates in a single step, making them suitable for electrical characterization.

Irradiation of p-type silicon with energetic light ions, such as protons and helium, introduces lattice defects which reduce or fully deplete the free carrier density of the irradiated

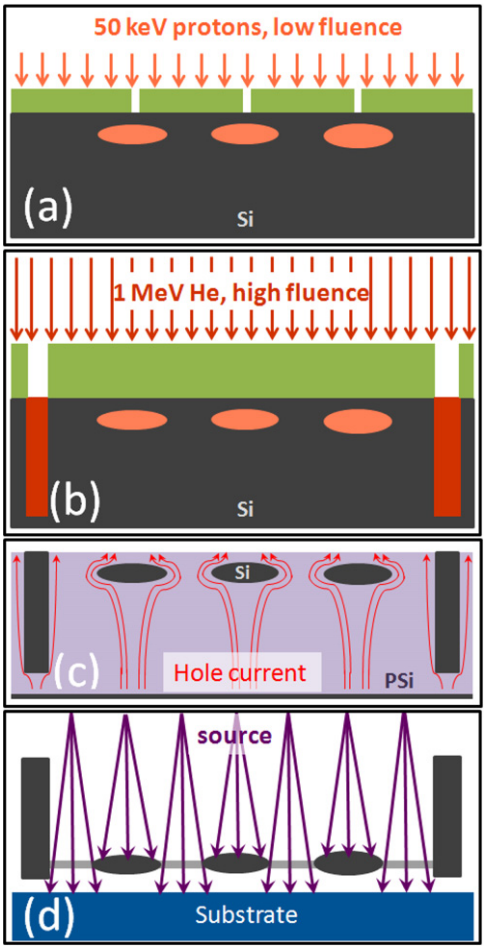


**Figure 1.** Schematic fabrication process for nanostencil masks. (a) Low fluence irradiation with 50 keV protons to form the nanoscale mask features; the ion end-of-range regions are shown in orange. (b) High fluence irradiation with 1 MeV helium ions to form the coarse, supporting mask structure; the orange bars show the full ion trajectories. (c) Anodization beyond the end of range of the helium ions. (d) After mask separation, it is inverted and used for pattern transfer, perhaps by using PLD deposition.

volume. Proton and helium ion energies of greater than 20 keV are above the Bragg peak of nuclear energy loss [35, 36], so their maximum rate of defect generation lies beneath the surface, close to their end-of-range depth, where the defect density is typically 10 to 20 times greater than it is close to the surface. These depleted regions remain as crystalline regions [37–46] and do not undergo porous silicon formation during subsequent electrochemical anodization. This process has been developed for a variety of applications in 3D silicon machining, silicon photonics, microelectromechanical systems, and photonic lattices, as reviewed in [42].

We have further developed this process by producing completely freestanding patterned silicon membranes that act as stencil masks. The schematic process is shown in figure 1. First, a 1 $\mu$m-thick polymethyl methacrylate (PMMA) photoresist is spin-coated on a 0.02 $\Omega$ cm p-type silicon wafer. Then, electron beam lithography is used to pattern an array of narrow line openings, as seen in figure 1(a), though other

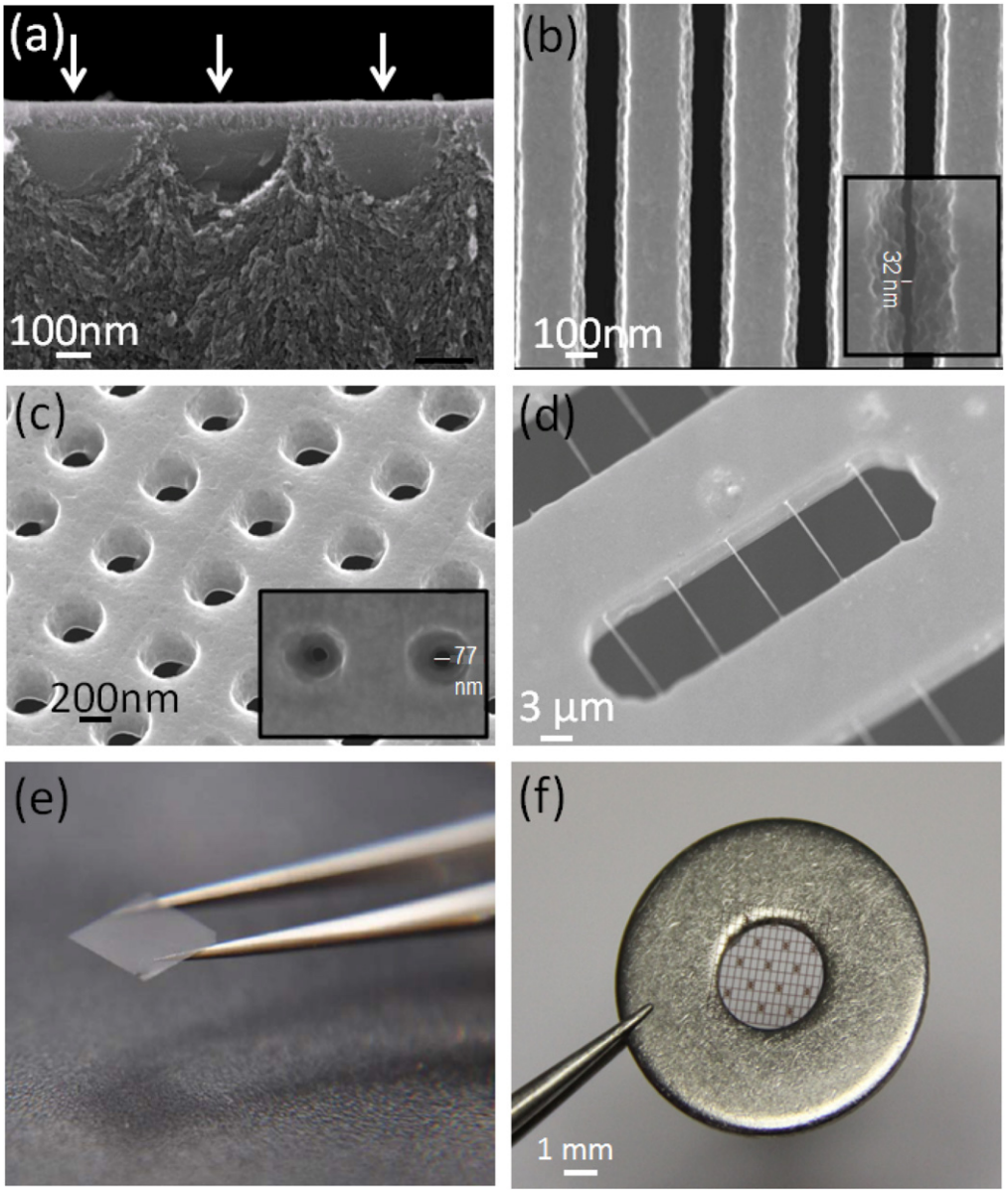


**Figure 2.** (a) Cross-section scanning electron microscope (SEM) of the silicon bars after irradiation with 50 keV protons, period of 550 nm; the irradiated surface areas are indicated by arrows. (b) SEM of a row of bars with a period of 650 nm, separated by a uniform gap of 100 nm; inset shows a gap of only 30 nm, with the same magnification. (c) SEM of a uniform array of holes with diameters of a few hundred nanometers; inset shows holes produced with diameters of ∼80 nm. (d) SEM of 150 nm-diameter bars, 8 $\mu$m long, supported by a 3 $\mu$m-thick structure. (e) and (f) Optical micrographs of a stencil picked up with tweezers and then mounted on a support.

shapes are easily incorporated. The resist is thick enough to fully stop 50 keV protons (a range of 0.8 $\mu$m in PMMA, 0.6 $\mu$m in silicon), so only exposed wafer surfaces are subsequently irradiated with a low ion fluence of $1 \times 10^{14}$ ions cm$^{-2}$. The orange ellipses in figure 1(a) indicate the ion end-of-range regions where the induced defect density peaks below the exposed surfaces. For optimal fluence, these fully-depleted regions remain as silicon bars during subsequent anodization, whereas the region above is anodized owing to its lower defect density. Anodization beyond the end-of-range depth results in a silicon bar completely surrounded by porous silicon, as shown in figure 2(a). Each bar may be elliptical or semicircular in shape, with a typical thickness around 400 nm, depending on the irradiation and anodization conditions.

Where required, wider supporting structures may be incorporated into the e-beam patterned resist, resulting in freestanding nanoscale bars held in place by orthogonal bars. However, since these e-beam patterned supports are of a similar thickness to the nanoscale bars, they do not provide sufficient rigidity to support them over large areas. Instead, the e-beam defined features are supported within the nanostencil using a second irradiation step prior to anodization, as seen in figure 1(b). The e-beam resist is stripped and the wafer surface coated with a 5 $\mu$m-thick photoresist. This is patterned with ultraviolet lithography and a mask aligner used to form a coarse grid structure comprising the exposed widths of 10 $\mu$m, with a period from tens to hundreds of microns, as required. The wafer is then irradiated using a high fluence of $2 \times 10^{15}$

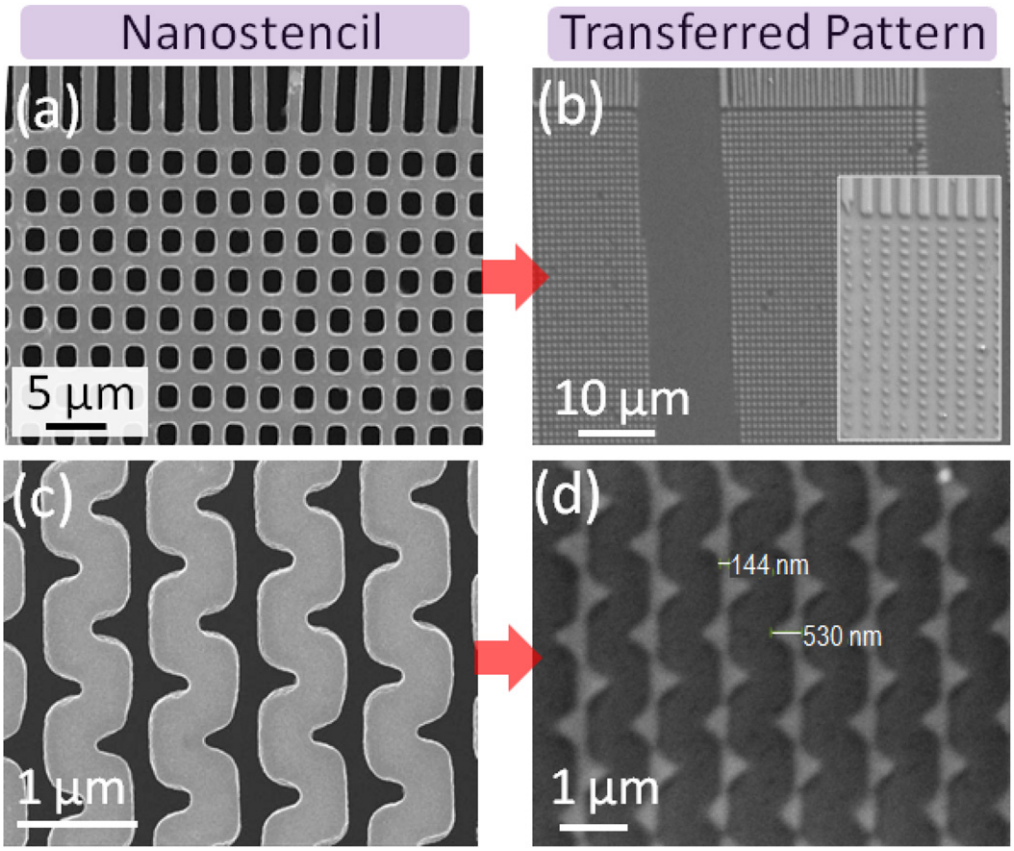


**Figure 3.** (a), (c) SEMs of nanostencil patterns. (b), (d) corresponding LAO pattern on an STO substrate.

ions $cm^{-2}$ by 1 MeV helium ions (a range of 3.5 $\mu$m in silicon). This ensures that anodization is fully stopped throughout the helium irradiated depth, as represented by the orange bars in figure 1(b). The range of the MeV helium ions defines the thickness of the coarse supporting structure or any coarse-scale features, ensuring that the final membrane is rigid enough to be handled and mounted. Both MeV helium and proton irradiation are performed using our large area irradiation facility [44], which can uniformly irradiate areas up to $1 \times 1$ inch square, with beam currents of hundreds of nanoamperes, giving the required fluences of $10^{14}$ to $10^{16}$ ions $cm^{-2}$ in an exposure time of a few minutes to one hour.

After irradiation, the thick photoresist is removed and the wafer is anodized using a current density of ~50 mA $cm^{-2}$ to a depth at which the high-energy helium irradiation regions are completely undercut, which typically requires an etch depth of 15 $\mu$m (figure 1(c)). The crystalline stencil, which is embedded in porous silicon, is removed from the silicon by one of two processes. First, the stencil can be removed by brief immersion in potassium hydroxide, which results in vigorous bubbling during dissolution of the silicon with an associated risk of damaging the nanoscale features. A brief thermal oxidation step at 800 °C for 10 min, followed by immersion in dilute hydrofluoric acid (HF), removes any remaining low porosity silicon clinging to the structure with no oxidation-induced stress. The second separation method involves annealing at 900 °C for 10 min to partially convert porous silicon to fully oxidized porous silicon [38], which is removed by immersion in dilute HF. This process produces little bubbling, so it has a low risk of damaging nanoscale features; however, care must be taken not to oxidize the porous layer at too high a temperature, or for too long, or the stencil can be permanently distorted by the formation of a highly strained, thick oxide layer which can bend the heated substrate, leading to dislocations that form in the crystalline nanostencil and remain in place after cooling. After separating the stencil from the substrate, it is mounted in a rigid frame for easy handling, as shown in figure 1(d). This mask can be directly used for deposition with processes such as pulsed laser deposition (PLD).

The minimum achievable gap between adjacent bars is ~100 nm, shown in figure 2(b). Smaller gaps down to 30 nm have been produced, as presented in the figure 2(b) inset, using either a smaller period between lines or a higher line fluence, but the sidewall roughness increases sharply as the gap is reduced, most likely due to the reduced anodization current density [47] as the gap becomes smaller. The minimum achievable uniformly etched gap also depends on the wafer resistivity; we have observed that fabrication of similar bars in higher resistivity (0.4 $\Omega$ cm) wafers results in a much larger minimum gap of ~700 nm. We also tried to produce smaller gaps in wafers of even lower resistivity (0.002 $\Omega$ cm), but this required a prohibitively large ion fluence to deplete the free carrier density enough to form silicon bars, with the likelihood of the surface polymer mask being distorted or even melted. Hence, in our experience, a resistivity of about

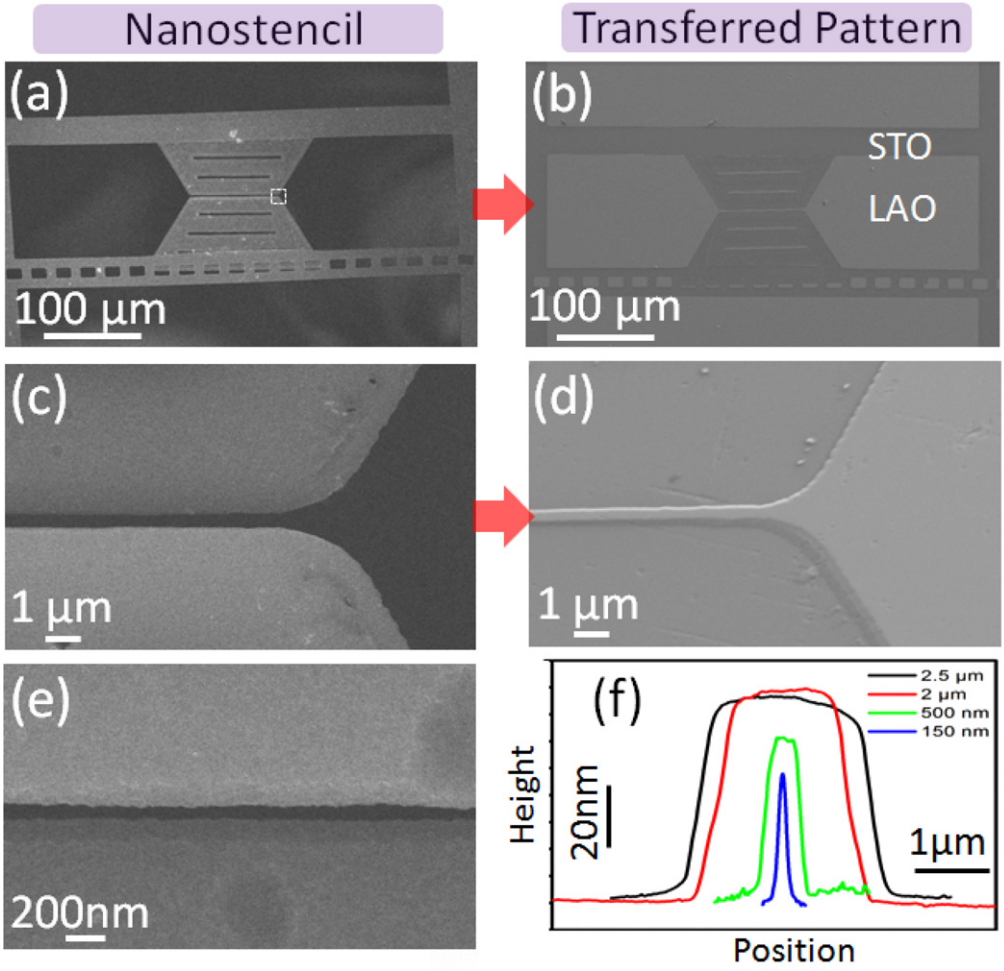


**Figure 4.** (a), (c), (e) SEM images of the nanostencil. (b), (d) corresponding transferred LAO pattern on STO. (f) AFM line scan profiles of LAO wires produced by different stencil channel widths, ranging from 2.5 $\mu$m to 150 nm.

0.02 $\Omega$ cm gives optimum results, allowing features such as circular holes with diameters down to 80 nm (figure 2(c)) and long, cylindrical bars with diameters of 150 nm (figure 2(d)). Figure 2(e) shows the stencil on tweezers, which allow it to be mounted on a support (like a washer) for further support if necessary (figure 2(f)).

It has been shown that amorphous LAO films deposited on STO even at room temperature lead to the formation of a two-dimensional electron gas at the LAO/STO interface. The origin of this electron gas has been unambiguously shown to arise from oxygen vacancies, as opposed to those that arise from polar catastrophe for which a crystalline interface is required [48]. Amorphous LAO was deposited on (001) STO substrates through such a silicon nanostencil via PLD at room temperature, with an oxygen pressure of $1 \times 10^{-5}$ Torr. The low oxygen pressure preserves the high directionality of the laser plume and renders pattern transfer less prone to blurring. Figure 3 shows various stencil patterns and the resulting deposited LAO patterns. Figures 3(a) and (b), respectively, show a large array of micrometer-size openings in a stencil and the corresponding matrix of transferred LAO dots with lengths of ~1.5 $\mu$m and a period of 3 $\mu$m. Figure 3(c) shows a stencil patterned with more complex, arbitrary shapes, which is possible because our method is independent of directional etching towards a particular crystallographic orientation. A pattern of zigzag lines with a gap width of ~200 nm was created, and figure 3(d) shows the corresponding LAO pattern where the sharp triangular shapes have a width of ~150 nm. These transferred patterns demonstrate that nanostencil lithography, in conjunction with PLD deposition, is capable of making simple, reliable pattern transfers over large areas.

An important feature of this fabrication process is that it readily allows the creation of a combination of features of widely differing sizes and membrane thicknesses, achieved using different irradiating energies to define the local mask thickness, as seen in figure 1. Large features are defined using high energy ions with ranges of several microns, such as 1 MeV helium, and nanoscale features defined using lower energy/range ions. We have successfully patterned LAO/STO-conducting nanowires with different line widths ranging from 2.5 $\mu$m to 150 nm, and investigated their transport properties. Figures 4(a), (c), and (e) show features of a stencil in which a 0.5 $\mu$m channel opening connects two hundred-micrometer-wide openings for the large electrode pads. The channel width can be made as wide as required (up to 2.5 $\mu$m in this case) and as narrow as ~80 nm, as shown in

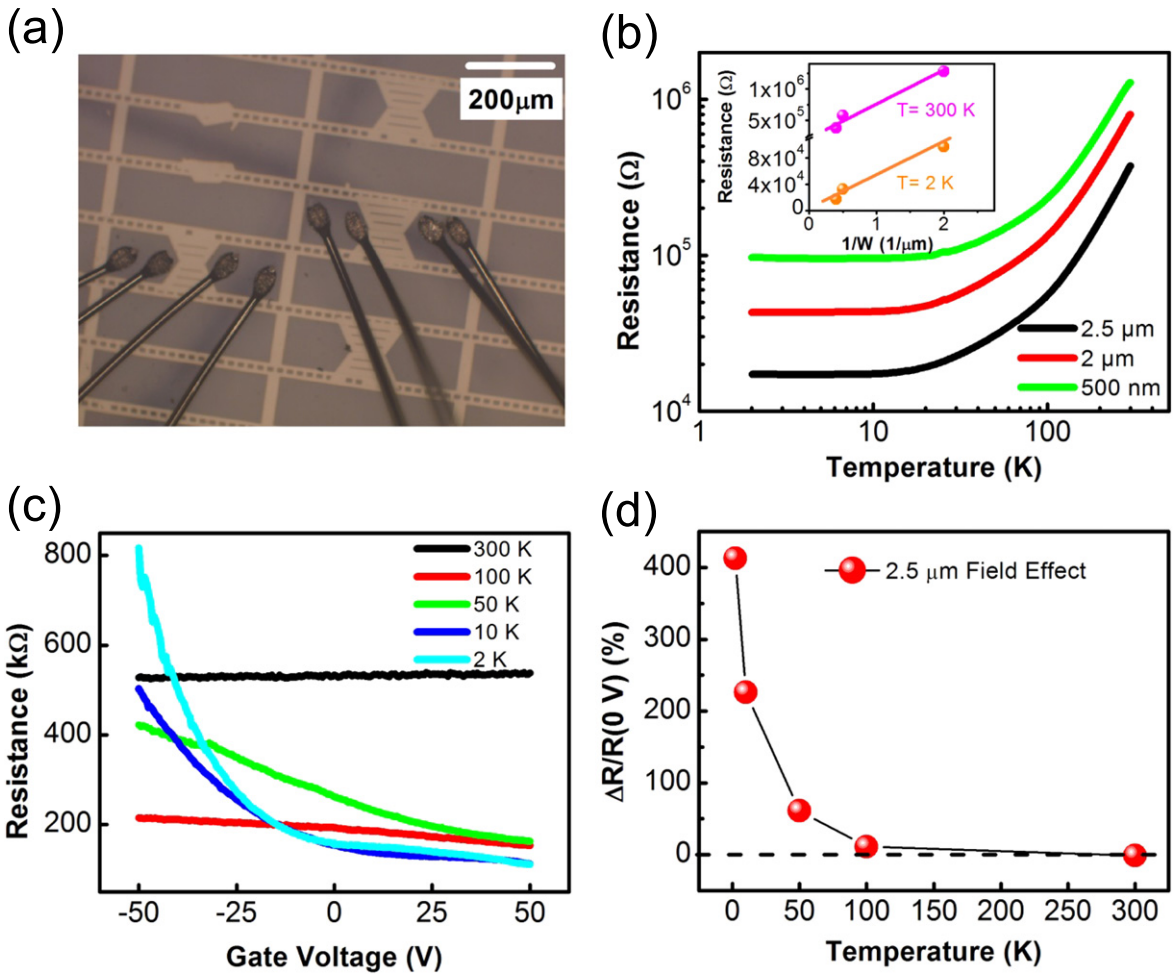


**Figure 5.** (a) Optical micrograph of transferred LAO with electrical bonds to the large patterned contact areas. (b) Resistance dependence on temperature for different width of LAO wires; inset shows the resistance of nanowires, which appear inversely proportional to the width of the nanowire at 300 and 2 K. (c) Electric field effect of 2.5 $\mu$m LAO wire resistance on the back gating voltage at 2 K for various temperatures. (d) Temperature dependence of field modulation at a fixed voltage.

figure 4(e). Figures 4(b) and (d) show the transferred 100 $\mu$m LAO nanowire and electrodes on an STO substrate; clearly the nanowire is very uniform. The nanowire topography profiles for different wire widths are shown in figure 4(f), as measured from atomic force microscopy (AFM) line scans. The nanowire edge remains sharp (100 to 200 nm) for channel openings down to 150 nm. For narrower openings (e.g., figure 2(e)), the transferred pattern was more blurred, probably due to a small gap between the stencil and the STO surface. We also note that the nanowire thickness depends on the channel width–for openings narrower than 2.0 $\mu$m, the thickness reduces.

The transport properties of the nanowires were measured using the four-probe method with aluminium wire bonding to the large pads, seen in figure 5(a). Figure 5(b) shows the resistance versus temperature dependence for nanowires with different widths. For a line width change from 2.5 $\mu$m to 500 nm, all nanowires remain fully metallic over the temperature range of 300 K to 2 K, which is consistent with thin film measurements. The resistance scales up with the decreasing nanowire width. The measured resistivity extracted from these curves is about $5.5 \times 10^{-4}\,\Omega$ cm, assuming the conducting channel of the LAO/STO interface is confined within several unit cells in the STO that are adjacent to the interface, which is slightly larger than the resistivity of reduced $SrTiO_3$ [48]. The value is expected due to the common origin of the oxygen vacancies in $SrTiO_3$. The scaling law, $R \propto W^{-1}$, holds at 300 K and at low temperature (2 K) for LAO/STO nanowires with different line widths, as shown in the inset of figure 5(b). Furthermore, the large electric field effect of the LAO/STO nanowire has been demonstrated through back-gating, using the STO as the dielectric. As shown in figure 5(c), the resistance of the 2.5 $\mu$m-wide wire strongly depends on the gate voltage across the STO. With a gate voltage of −50 V at 2 K, the resistance changes by more than 400%, which is much larger than the modulation effect when the LAO is in thin-film form at 2 K [49, 50]. This demonstrates the potential of field effect devices based on an LAO/STO interface, even if the effect diminishes at room temperature (figure 5(d)). Clearly, the field effect scales with the dielectric property of the STO substrate as a function of temperature [51, 52].

In summary, we have demonstrated the versatility of nanostencil lithography based on fully crystalline silicon

masks for nanopatterned oxide growth using PLD. With its ability to produce arbitrary shapes in a stencil mask architecture comprising gaps that range from less than 100 nm to greater than 100 $\mu$m, multiscale lithography is achieved in a single lithography step. LAO/STO nanowires with simultaneous deneeposition of electrical conduct pads greatly simplify the fabrication process of LAO/STO-based devices. LAO/STO nanowires not only preserve conductivity, but also possess an enhanced field effect. The large modulation achieved with a moderate gate voltage demonstrates the potential for field effect devices based on an LAO/STO interface. We conclude that stencil lithography incorporating multiple feature sizes in a single mask shows great potential for the future development of oxide electronics.

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