Fabrication of 3D photonic components on bulk crystalline silicon

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Abstract: We have fabricated three dimensional photonic components such as waveguides and beam splitters from crystalline silicon using a process based on one or more ion irradiation steps with different energies and fluences, followed by electrochemical anodization and thermal annealing. We first demonstrate the fabrication of multilevel silicon waveguides and then extend this process to make multilevel beam splitters, in which three output waveguides are distributed over two depths. The dimensions of the waveguides can be defined within a range from 0.5 μm to several micrometers simply by varying the ion beam fluence.

OCIS codes: (130.3990) Micro-optical devices; (220.4610) Optical fabrication; (230.1360) Beam splitters; (230.4170) Multilayers.

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1. Introduction

Several new technologies, e.g. 3D memories, many-core processors, are being developed to overcome present limitations of semiconductors and planar microelectronics. 3D layer architectures would reduce restrictions by avoiding physical crossings as well as reducing the traditional limitations of limited physical chip area. 3D multilevel photonics would also provide engineers with a new dimension in which to work, enabling denser, more complex networks. For example [1], describes studies toward realizing a system integration platform based on photonics and electronics convergence. Furthermore, there is great interest in developing photonic optical interconnects to enhance the bandwidth and reduce power consumption in multi-core computing systems [2].

To achieve such vertically stacked, multilayer, 3D architectures, it may not be possible to use the traditional, optimized materials such as bulk, crystalline silicon. Therefore, researchers are looking at other routes to achieve the 3D integration. For example, using a wafer bonding approach [3, 4], devices are fabricated on two separate chips, then the two aligned chips are attached. Chemical vapor deposition (CVD) [5] can be used for deposition of organics to make stacked polymer devices, or plasma enhanced chemical vapor deposition (PECVD) [6] can deposit multilayer Si_3N_4 and SiO_2 structures. Similarly, epitaxial growth [7] can also be used to fabricate heterostructure devices layer by layer using semiconductors such as SiGe and GaAs. Another route is by using a modified SIMOX process [8, 9], involving patterned oxygen implantation. In previous work [10], we fabricated vertically-stacked waveguide couplers based on a SOI wafer. Here we demonstrate a process for fabricating 3D photonic structures only using bulk, crystalline silicon with a single etching step.

2. Fabrication process applied to 3D waveguides arrays

We have developed a micro- and nano-machining process in p-type crystalline silicon based on using high-energy ion beam (a few hundred keV) irradiation with subsequent electrochemical anodization [11–14]. High energy ions can penetrate many micrometers into silicon and create defects along their trajectories. The net effect of these defects is to increase

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the resistivity of the irradiated volume so that a smaller hole current flows through it during anodization, so reducing the rate of porous silicon formation. For a high ion fluence, the rate of porous silicon formation throughout the irradiated volume is reduced to zero as the entire flow of hole anodization current is deflected away from the defect regions, leaving them unetched as fully crystalline regions surrounded by porous silicon.

Since most ion induced defects are located close to the ion end-of-range, for a low fluence irradiation only the end-of-range region remains unetched while regions closer to the surface become etched. The ion range, is a well-defined function of the ion energy, so by choosing ions with different energies, different end-of-range depths can be incorporated. Thus, by varying the ion energy and using low fluences within an irradiated volume, it is possible to directly fabricate 3D microstructures on silicon comprising unetched end-of-range regions. See [15, 16] for an account of our work in 3D microfabrication using direct writing with a focused proton beam. However, this direct writing approach is not appropriate for upscaling to large volume production of 3D photonic components, so we have developed a facility [17] in which a high beam current of about 1 μA is used to uniformly irradiate large sample areas. This large area irradiation facility is used here to build up a pattern of three-dimensional micro- and nano-scale damage over large patterned areas of crystalline silicon, in order to fabricate multilevel components such as linear waveguide arrays and 3D splitters in conjunction with photolithography. The most suitable wafer resistivity for this process is p-type, between 0.5 to 10 Ω·cm [11]. More highly-doped wafers result in excessive propagation losses due to scattering from free carriers. In lower-doped wafers the electrochemical anodization process cannot be easily tuned to distinguish between the irradiated end-of-range region and the region closer to the surface containing a lower defect density, making 3D machining difficult, as well as a tendency to produce macroporous silicon [18].

Figure 1(a) shows a schematic diagram of the irradiation procedure using a single irradiation step. Firstly, a p-type, 0.5 Ω·cm silicon substrate is coated with a patterned photo-resist of thickness less than the ion beam range. A proton beam energy of 650 keV is used to irradiate a large area through this patterned photo-resist. The beam which irradiates the exposed surfaces passes directly into the silicon and generates a high defect density region at the end-of-range, whereas the beam portion which is incident on the polymer has its energy reduced in passing through it, so the end-of-range peak in the silicon is at a shallower depth. The range for 650 keV protons at unmasked regions is 9 μm as calculated using SRIM [19]. At masked regions these ions penetrate the 7 μm thick photo-resist and stop at a depth of 3.5 μm below the surface. After a single energy beam irradiation with a fluence of $5 \times 10^{13}/\text{cm}^2$, electrochemical etching is carried out, resulting in two different layers of waveguides at the end-of-range regions which are surrounded by porous silicon, as the SEM images show in Figs. 1(b) and 1(c). The waveguide size is determined by the irradiated ion fluence, and the period and gap size of the photoresist, while the depth is determined by the resist thickness and ion beam energy.

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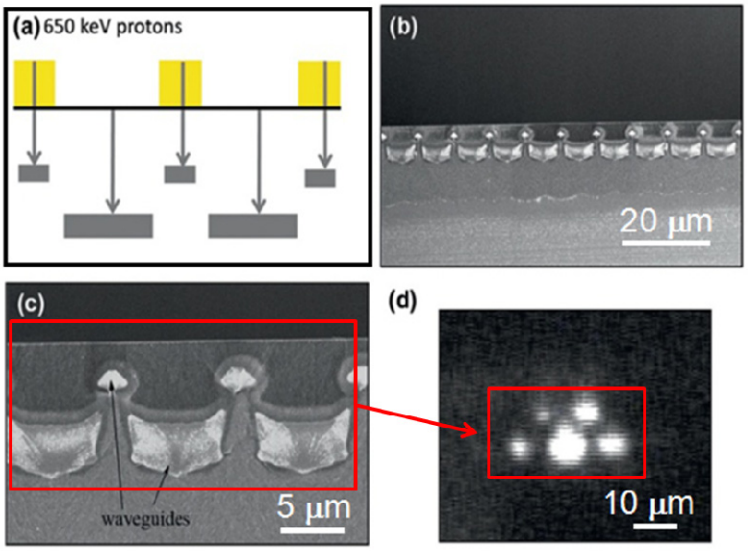

Fig. 1. (a) Two-levels of waveguides formed by single energy irradiation through a patterned photoresist (yellow areas). (b), (c) cross-section SEMs of this structure after irradiation and anodization (d). Corresponding output image from cross-section by simultaneously coupling infrared light into all the waveguides

This process may be easily extended to add more layers of waveguides, as shown in Fig. 2, where a second irradiation with 300 keV helium ions (range of 1.3 µm in silicon), was performed after a similar first irradiation step with 650 keV protons. The lower energy helium ions cannot pass through the 7 µm photo-resist. The cross-section SEM images show the three different layers of silicon waveguides formed at the end-of-range depths, with the bottom and middle levels of waveguides formed by a 650 keV proton fluence of $5 \times 10^{13}/cm^2$ and the top level of waveguide formed with a 300 keV helium ion fluence of $1 \times 10^{13}/cm^2$.

Figures 1(d) and 2(d) show the corresponding output image for laser coupling of the two and three level system. During the optical test, the input infrared laser beam was defocused so that many vertically stacked waveguides can be coupled at the same time. The larger silicon waveguides in the top and bottom rows confine light. However, in Figs. 2(b) and 2(c) silicon waveguides of less than 1 µm in width and height are observed in the middle row of the three level system, their size depending on the period and width of the photoresist pattern and on the fluences used. There is no detectable light transmitted through the waveguides in this row, partly because their size is small, less than one tenth of the size of the other two layer waveguides, the surface roughness is high (~10 nm) and ion induced defects present from the irradiation process act as scattering centers.

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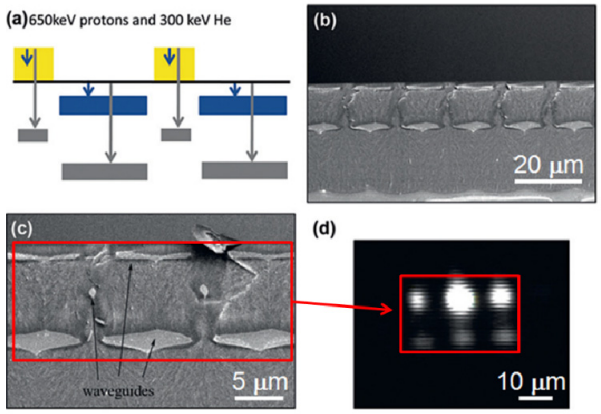

Fig. 2. Level system formed by double energy irradiation through a mask (yellow areas). The end-of-range regions of the 650 keV protons (grey areas) and 300 keV helium ions (blue areas) is shown. (b),(c) cross-section SEMs of this structure after irradiation and anodization (d). Corresponding output image by simultaneously coupling light into all the waveguides.

We have previously studied the effect of high temperature oxidation on reducing propagation losses in 2D waveguides fabricated using this process [12], following the work described in [14,15]. After oxidation at around 1000°C for three hours we find that the surface roughness may be significantly reduced to around 1 nm. This, coupled with a removal of ion induced defects, resulted the waveguide propagation losses reducing from around 10dB/cm to around 1 dB/cm. In view of this, we believe that by using this technique, more levels of waveguides can be also achieved. 3D arrays of sub-micron waveguides can be fabricated, once issues of high propagation losses due to surface roughness have been addressed. Further optimization of the waveguide profile can be achieved by improving the quality of the photo-resist mask.

3. 3D Beam splitters

For on-chip photonics, a beam splitter is usually a component comprising one waveguide input and two waveguide outputs. There are two main types, according to their functions. First, optical power splitters which simply split an incident light beam into two equal outputs [22, 23], which is critical in creating modulators, interferometers and multiplexers. Second, on-chip polarization splitters which can give polarization dependent outputs; these are key components of integrated photonic circuits that consist of polarization dependent devices [24–27]. Most of them are based on SOI wafers and are 2D planar structures. With a modification of the fabrication process described in section 2, we have fabricated 3D splitters on crystalline silicon. This process involves irradiation with two ion beam energies, but requires an additional step whereby a different polymer resist pattern is deposited between the first and second irradiation step so that different patterns can be fabricated at each layer depth.

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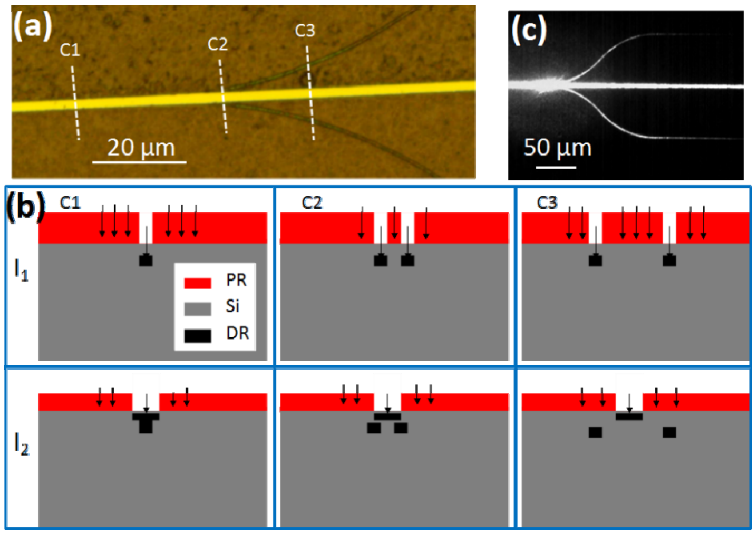

Fig. 3. (a) Optical micrograph of the splitter. (b) schematic of the ion beam irradiation patterning process: I_1, the first irradiation to pattern the two lower waveguides; I_2, the second irradiation to pattern the upper waveguide. (c) Plan view of scattered light image in TE mode.

Figure 3 shows an optical micrograph of a fabricated 3D beam splitter, and a schematic of the two irradiation steps used to pattern two layer depths of waveguides with two different ion energies. For the first irradiation step the splitter layout in the lower level was patterned using standard UV photolithography of a 5 µm thick AZ 9260 photoresist which was spin-coated on 0.3 Ω·cm p-type wafer. The wafer surface was then irradiated over a large area with a beam of 250 keV protons, which have a range of ~2.4 µm in silicon. The photoresist is thick enough to stop the beam irradiating the silicon wafer at the covered regions, so defects are only created at the exposed regions. The irradiation fluence of 8×10^{13} ions/cm^2 results in a high defect density at the end-of-range which is sufficient to prevent this volume undergoing anodization.

After the first irradiation, we used physical vapor deposition (PVD) to deposit a 30 nm thick gold layer on the surface. When the first step photoresist was removed, the gold pattern remained on the silicon surface and was used as an alignment mark for the second irradiation step. A second photoresist layer of 1 µm thick SU8 2000.5 was spin-coated, and an aligned UV lithography step was carried out for the second layer patterning. A lower beam energy of 50 keV protons (range of 800 nm in the photoresist) was then used to irradiate the sample with a high fluence of 2×10^{15}/cm^2, sufficient to fully stop subsequent PSi formation within the irradiated volume and to form the upper level of patterned structures.

After removing the second step photoresist, the wafer was electrochemically etched in 24% HF with a current density of 60 mA/cm^2 for 1 minute to make a porous silicon layer of ~2.4 µm thick. The porous silicon layer was then removed in KOH solution, and the wafer was electrochemically etched for the second step with a current density of 40 mA/cm^2 for 5-6 minutes to make a porous silicon layer of ~10 µm thickness. Finally, the wafer was annealed in vacuum at 500þC for 9 hours and 950þC for 1 hour to anneal out the beam induced defects without significantly reducing the waveguide cross-sectional area by oxidation since they are already thin (0.5 µm) [10, 12]. The width of the waveguides was designed as 3.5 µm which is wide enough for easy coupling of light into them.

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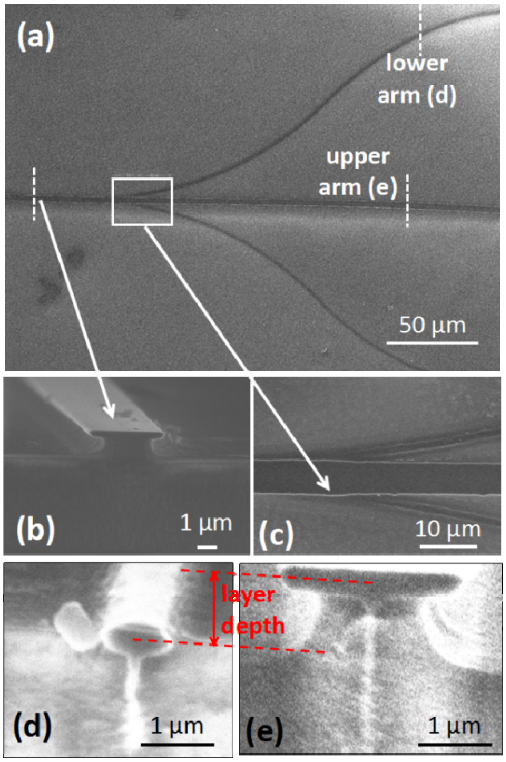

Fig. 4. SEM images of the splitter (a) top view of the structure, and cross section views of (b) the input, (d) the lower, and (e) the upper waveguides; and (c) a high resolution top view at the splitting portion.

Figure 4 shows SEM images of various portions of the 3D splitter in which the lower level waveguides are curved. The figure shows curved lower waveguides and the upper waveguide designed as straight from the main waveguide input. From the top view of the splitter, we observe the three waveguides located at different layers. From the cross section SEM in Figs. 4(d) and 4(e) we measure a depth difference between the two layers of ~1.9 µm. In this example, cross section SEMs show that the lower waveguides are much narrower (width × height of ~0.7 × 0.5 µm^2) than the upper one (~4.1 × 0.5 µm^2), even though their widths were designed to be the same. This is due to the low fluence (8 × 10^{13} ions/cm^2) used for irradiation of the lower waveguides, resulting in only a small volume containing a sufficiently high defect density remained during anodization.

Characterization of the splitting behavior was carried out with a light wavelength of 1.55 µm. Infrared (IR) images of the light coupling in the 3D splitter are shown in Fig. 3(c). We observe light coupled from the main waveguide into three output waveguides which are located on two different layers. We denote the lower waveguides as L_1 and L_2, and the upper as U. From the output power we measured a splitting ratio of L_1: (U = 1.0): L_2 as 0.05: 1: 0.16 for a TE mode input, and 0.03: 1:0.13 for a TM input. The splitting ratios of the lower ones are small, arising from their small dimensions which also give a high propagation loss of ~31.2 dB/cm, measured from the scattered light along the propagation. The propagation loss of the upper waveguide, measured the same way, is ~10.1 dB/cm.

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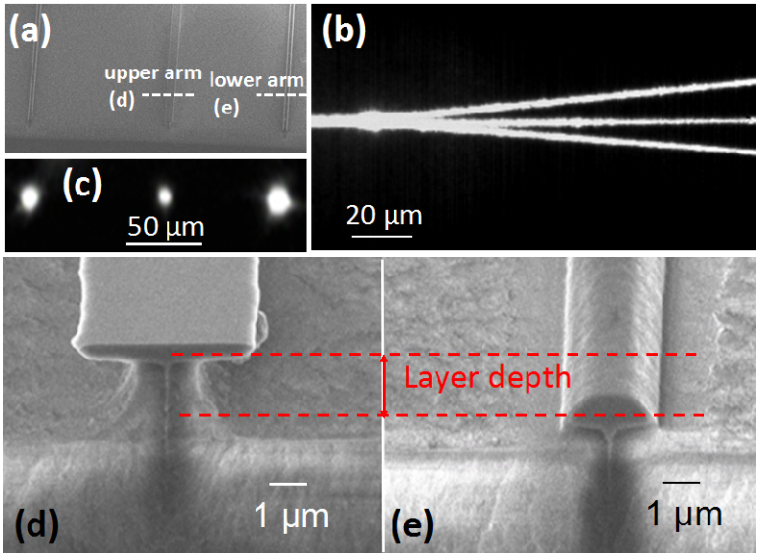

Fig. 5. (a) SEM of the three output ports; (b),(c) plan and cross-section view of light splitting. Note that (a) and (c) are on the same scale. SEMs of (d) upper and (e) lower output waveguides.

Using the same process as above we also fabricated a different design in which the lower waveguides were straight, inclined at an angle of 5þ to the straight upper waveguide, Fig. 5. We increased the irradiation fluence for the lower waveguides to 1×10^{14} ions/cm^2 while the fluence for the upper waveguide remained the same. As a result of the higher fluence the dimension of the lower waveguides was increased to ~2.1 × 0.9 µm^2, Fig. 5 (e). Now the splitting ratio is much more uniform, see Fig. 5 (b), compared to Fig. 3 (c). Figure 5 (a) shows the three output ports of the three waveguides, and Fig. 5(c) the output light emerging from them. The splitting ratio in this case was measured as L_1: U: L_2 = 2.3:1:1.8 for TE mode, and the propagation loss of the lower waveguides decreased to ~6.7 dB/cm as a consequence of their larger cross-section.

Table 1. Relationship between the proton fluence used to create the waveguides, their resulting dimensions, losses and splitting ratios.

For lower output waveguides			Measured	Simulation
Irradiation fluences (ions/cm^2)	Dimensions (µm^2)	Losses (dB/cm)	Splitting Ratios for TE (L_1: U: L_2)	
8×10^{13}	0.7 × 0.5	31.2	0.05:1: 0.16	0.22:1:0.22
1×10^{14}	2.1 × 0.9	6.7	2.3:1: 1.8	2.7:1:2.7
2×10^{14}	3.4 × 1.4	4.2	3.7:1: 2.9	3.1:1:3.1
3×10^{14}	3.8 × 1.8	3.4	10.1:1: 9.3	10.1:1:10.1

With a higher irradiation fluence used for the lower waveguides, their dimension increases, as shown in Table 1. As a result, the splitting ratio is increased and the propagation loss is reduced. There are two reasons for the lower propagation loss with higher fluence. One is that thicker waveguides confine more light modes, the other is that a higher fluence results in a lower surface roughness [28].

Simulated values of the splitting ratios were computed using the RF module in the COMSOL 4.2 software package [29]. The input is set as the fundamental TE0 mode of the waveguide at a wavelength of 1550 nm. The refractive indices of Si and porous Si are set to be 3.45 and 1.5, respectively. The dimensions are set according to the measured results. The splitting ratios varies according to the dimensions of the output waveguides. The two lower waveguides were designed to be identical and symmetrical, so their splitting ratio should be

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the same and similar to the simulated values in Table 1. However, the measured results exhibit differences. In general they are close to the simulated values for the three higher fluences, but exhibit significant differences from one side to the other of the two waveguides. We believe that this arises from a slight misalignment during the fabrication process, resulting in the upper waveguide not being exactly located between the lower two. The misalignment accuracy is less than 1 μm, limited by normal UV alignment during fabrication, so it is logical that the smaller waveguides produced with low fluences are more strongly influenced by any misalignment. This could be reduced by using a more accurate alignment process or by using deep UV or E-beam lithography to achieve better control over the dimensions and alignment of the waveguides. We consider that the sharply increased waveguide propagation loss measured at the lowest fluence arises from a combination of reduced waveguide dimensions and increased surface roughness, as explained above.

4. Conclusion

We have presented the first 3D photonics components fabricated on bulk silicon. We have fabricated 3D arrays of waveguides and 3D splitters in two layers with two steps of irradiation with different ion energies. Successful light coupling into three output waveguides in two layers of the splitters was observed. The splitting ratios mainly depend on the dimensions of the waveguides in the two layers which could be controlled by the energy and irradiation fluence of the ion beam.

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