NATIONAL UNIVERSITY OF SINGAPORE

HONOURS THESIS

Creation of local band gap in bilayer graphene

Author:
NGUYEN Duy Quang

Supervisor:
Jens MARTIN

Abstract

Ever since its theoretical prediction [1–3], opening a band gap in graphene by an external electric field has been an emerging trend in research [4–9]. Recent achievements in graphene band gap engineering include the opening of a tunable bang gap of size up to 250 meV [5, 6, 9] and the formation of a quantum dot in bilayer graphene [4]. These experiments provided a proof-in-principle that a bang gap can be opened in bilayer graphene. Building on the previous experiments, we propose the fabrication of a locally gated device which has a set of local back gates instead of one global back gate and, thus, avoids the problem of unwanted induced charges. Here we report two new fabrication processes for a locally gated device: one involving LOR-A (MicroChem) and one involving hydrogen silsesquianone (HSQ). Electrical characterisations of electron beam exposed HSQ as a dielectric were performed. The devices fabricated with electron beam exposed HSQ show high durability, withstanding voltages up to 20.0 V at room temperature ($T \approx 25^{\circ}\mathrm{C}$) and displaying resistance in the order of 10 GΩ.

Contents

I. INTRODUCTION

Graphene, a crystalline structure of carbon with a thickness of a single or a few layers of atom, is an interesting material with very exciting properties. Being only a few atomic layers thick, graphene is both light and almost transparent. Its measured Young's modulus ranges from 0.5 to 1.0 TPa [10, 11], indicating high mechanical strength. In terms of its electronic properties, graphene can display charge mobility up to 10,000 $cm^2V^{-1}s^{-1}$ at room temperature - roughly ten times that of silicon [6]. Harnessing these highly promising properties of graphene, among other excellent qualities, has been the main motivation for research in "graphene electronics". However, making graphene into a working electronic device has its own challenges. First among all is the lack of a band gap in graphene. Without an insulating state, a graphene-based electronic device cannot be switched off by uisng control voltages [6, 12].

Graphene band gap engineering has, hence, been an emerging trend in research [4–9]. Here we focus on studies by Oostinga *et al.* (2007) [6], and more recently by M. T. Allen et al. (2012) [4], who demonstrated that an external electric field can induce a tunable energy gap up to 250 meV by breaking the layer symmetry in bilayer graphene. Building on their successes with gated bilayer graphene devices, in this project, we propose adding one further fabrication step, incorporating a set of local back gates in addition to the local top gates in a device which may be called a locally gated graphene device. Having the local gates in a device allows us to avoid the unwieldiness of having a global back voltage while affording us more control over the local band gap structures of the bilayer graphene device.

The primary aim of this project is to establish a fabrication procedure for a locally gated graphene device. This project report is organised as follows. Section II gives the research background and explains the motivation for the project. The experimental set-up and findings will be presented and discussed in section III. The electrical characterisations of the e-beam exposed HSQ deposits will be presented in Section IV. Section V will discuss the unresolved issues faced in the project and the works planned for the future. Section VI will conclude the report.

II. BACKGROUND AND MOTIVATION

The possibility of opening an energy band gap in bilayer graphene was predicted theoretically by McCann in 2006 in his paper on asymmetry gap in the electronic band structure of bilayer graphene [2, 3]. In 2007, G. Giovannetti *et al.* performed density functional calculations and also showed it would be possible to open a substrate-induced band gap in monolayer graphene on hexagonal boron nitride (BN) [1]. As noted by Oostinga *et al.*, a substrate-induced band gap, while theoretically possible, is not a viable option in practice as the technology requirements still prove too challenging [6]. A simpler method to open the band gap is by applying an external electric field that is perpendicular to the plane of the graphene sheet.

Following the theoretical predictions, Oostinga *et al.* in 2007 demonstrated that an energy band gap up to 10 meV can be opened by bilayer graphene [6]. Subsequent experiments showed that a tunable band gap up to 250 meV can be achieved by applying perpendicular external electric field on bilayer graphene [5, 9, 13]. A recent study by M. T. Allen *et al.* in 2012 demonstrated field-induced quantum confinement, which resulted in formation of a quantum dot, in suspended bilayer graphene [4].

In each of these experiments, a major constraint arises due to the global back gate: the effect of a voltage applied to the global back gate will be felt everywhere on the substrate. This results in the coupling of the electric field strength E in the compensated regions (areas of the sample covered by a top gate) and the induced charge carrier density n in the uncompensated regions (areas of the sample not covered by a top gate and, hence, under the influence of the global gate alone) as shown in Figure 1. Though this problem can be overcome by finding a ratio between the local top gate voltage V_t and the global back gate voltage V_b that maintains zero charge carrier density for the compensated regions [4, 6], we argue that it is far simpler and more advantageous to decouple E and n by constructing local back gates.

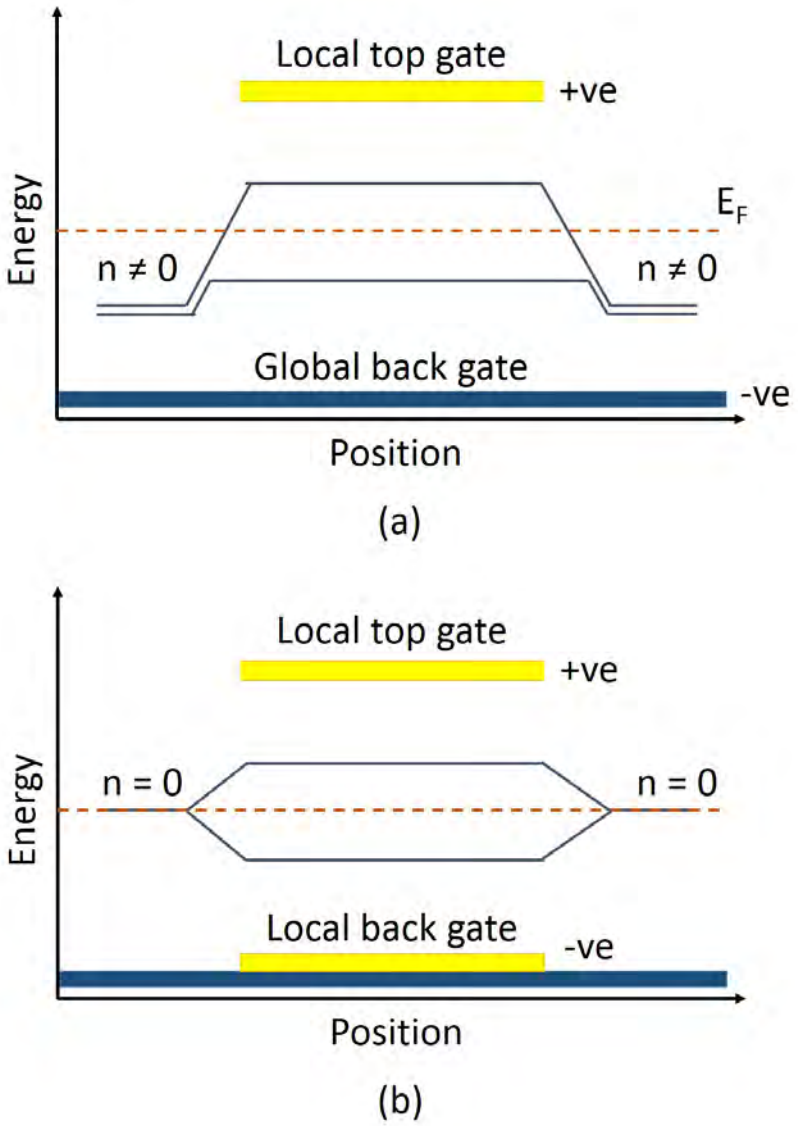


Figure 1: (a) Energy diagram for a device with the substrate as the global back gate. The electric field strength E between the top and back gates depends on the voltages (V_t and V_b respectively) applied to them and the thickness of the dielectric that separates each from the bilayer graphene. The uncompensated regions are also under the influence of the back gate voltage and charges may be induced (charge density $n \neq 0$). Finding a suitable ratio between V_t and V_b may decouple E and n. (b) Energy diagram for a locally gated device. The local electric field is contained between the local gates, preventing charges from building up in adjacent regions on the bilayer graphene crystal.

The aim of this project is to establish a suitable fabrication process for a graphene device with local gates. The ultimate goal is build one such device (Figure 2). As such, the scopes

of this project include testing and optimising laser lithography and e-beam lithography recipes, identifying suitable dielectric materials for use in the actual device, and carrying out electrical resistivity measurements to characterise the dielectric material chosen. The experiments that were carried out and the experimental findings are presented and discussed in the next section.

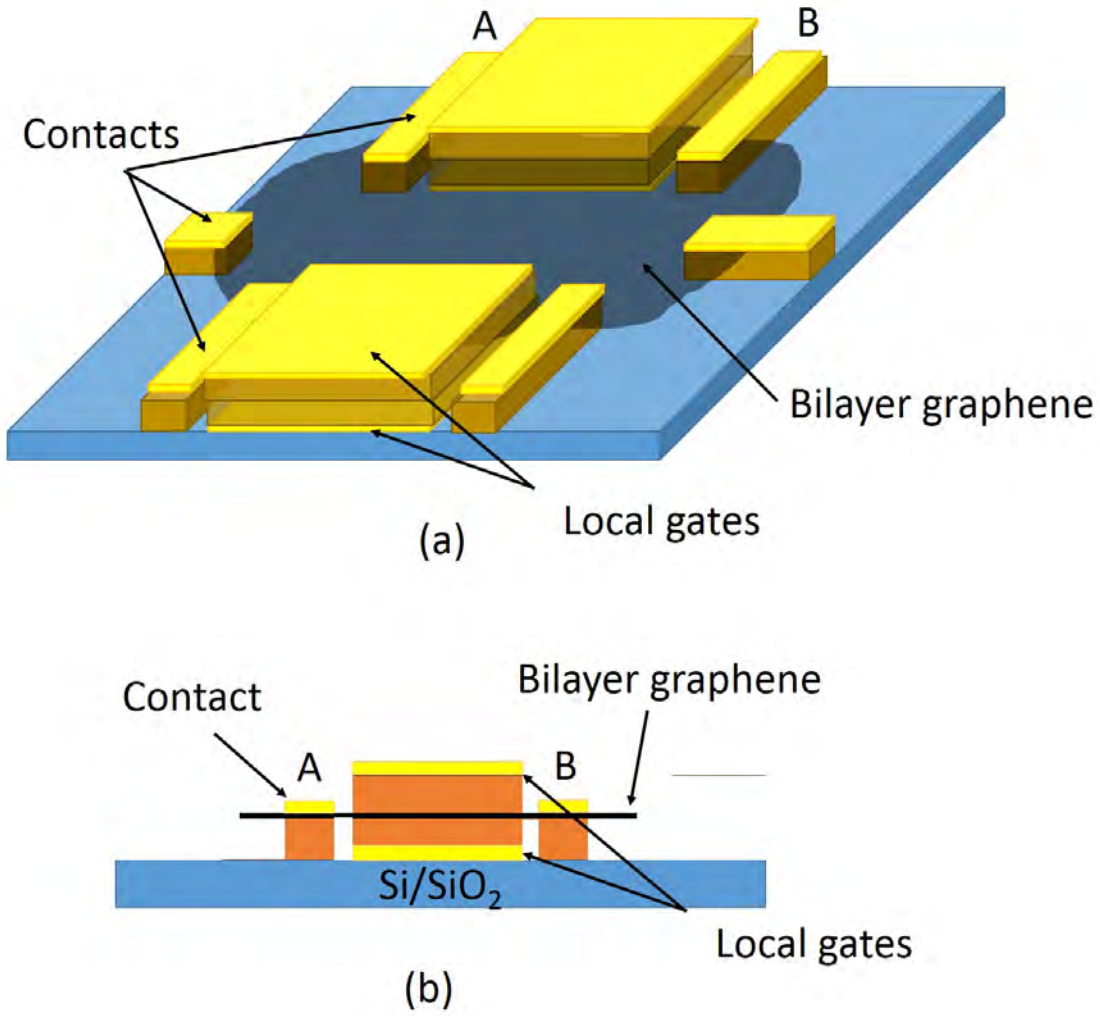


Figure 2: (a) Schematics of a simple locally gated graphene device with electrical contacts and suspended bilayer graphene. Electron transport disorders due to rugged edges of the bilayer graphene crystal are avoided as electrons are forbidden in regions with band gap opened by the local gates. (b) Diagram shows the cross section between A and B.

III. FABRICATION PROCESS OF LOCALLY GATED DEVICES

A. Design of the test device

As mentioned in Section II, the scopes of the project include establishing a fabrication process of a locally gated device and characterising a suitable insulating substance to be used as a dielectric in a graphene device. To address these aims, the following test structure (Figure 3) was designed. There are two reasons for doing this. Firstly, establishing a fabrication process for the test device will pave the way for a fabrication process for an actual graphene device. Secondly, the test device will be used to perform electrical measurements of the insulating material sandwiched between the local gates. The test device has been given a structure such that electrical measurements of different areas of the dielectric, under different geometries as well as top and back gates arrangements, can be documented.

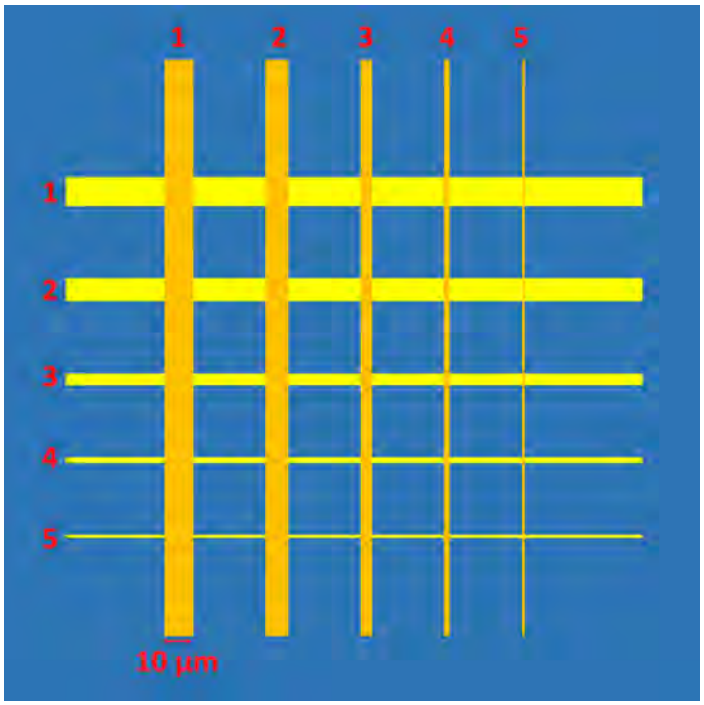


Figure 3: The design of the test device structure. The top (vertical) gates sit on top of the back (horizontal) gates. Between them is a layer of insulating material. The criss-crossing patterns and the different gate widths are designed so that electrical measurements of various areas of the insulator, subject to different geometries and top and back gates arrangements, can be performed

B. Process overview

Figure 4 below shows an overview of the works that have been done in this project. The section will follow closely the flow in the diagram. We will first report the fabrication process of the local back gates using electron beam (e-beam) lithography with PMMA resists. Next, we present our findings for the suitable dielectric substance for use in a locally gated graphene device. Here we also report the challenges faced, the failures that occurred, and the methods used to circumnavigate these problems. Lastly, we will report our electrical resistivity measurements that were performed for the e-beam exposed HSQ deposits.

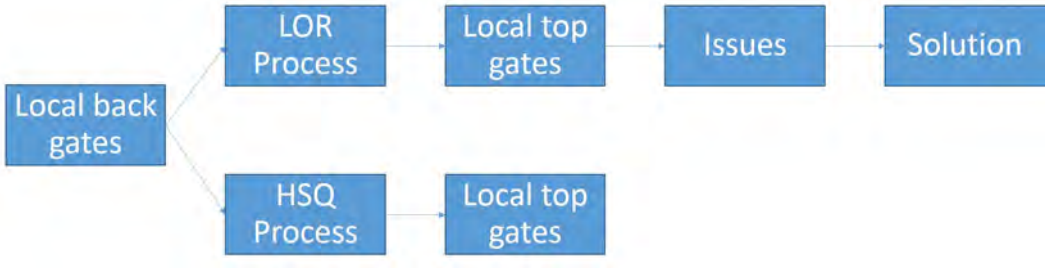


Figure 4: Overview of project work

C. Fabrication of the local back gates

1. *E-beam lithography recipes*

The fabrication of the local back gates on the substrate was done by applying the e-beam lithography process. PMMA 950 A5 was used as the main e-beam resist. Two different recipes were followed and they are summarised in Table I.

2. *Issues with metalisation and lift-off process*

Both recipes yielded well-defined patterns for the local back gates. Nevertheless, the lift-off process after metallisation proved to be difficult with the standard recipe. Typically, immersion in hot acetone at 65°C for about 45 minutes was required to uplift the metal layers from the substrate. Even so, one would still need to squirt acetone onto the substrate to create disturbances in order to completely remove the metal flakes. It was found out that cold acetone at room temperature

	Standard recipe	Modified recipe
E-beam resist(s) used	One layer of PMMA 950 A5	2 layers of PMMA 495 A3 followed by one layer of PMMA 950 A5
Spin-coating speed(s)	4000 rpm for 80 sec	2000 rpm for 60 sec for PMMA 495 A3, 4000 rpm for 80 sec for PMMA 950 A5
Pre-bake temperature	180°C for 4 min	No pre-baking for first PMMA 495 A3 layer, 170°C for 5 min for second PMMA 495 A3 layer, 180°C for 4 min for PMMA 950 A5 layer.
E-beam dose	150 μC/cm^2	450 μC/cm^2
Development	MIBK:IPA 1:1 for 30 sec then rinsed in IPA for 30 sec	MIBK:IPA 1:3 for 25 sec then rinsed in IPA for 25 s

Table I: A comparison between the standard recipe and the modified recipe used for the fabrication process of the local back gates

would not uplift the metals even when the sample was left submerged overnight. The use of the ultrasonic bath set for 1 - 2 minutes was needed for the lift-off process in cold acetone.

The difficulty faced in the lift-off process was partially overcome by following the modified recipe (Figure 5). With the modified recipe, the lift-off process in hot acetone at 65°C was shortened to 5 minutes, while that in cold acetone would take 45 minutes. Agitation by squirting acetone onto the substrate is still needed in order to completely remove the metal flakes.

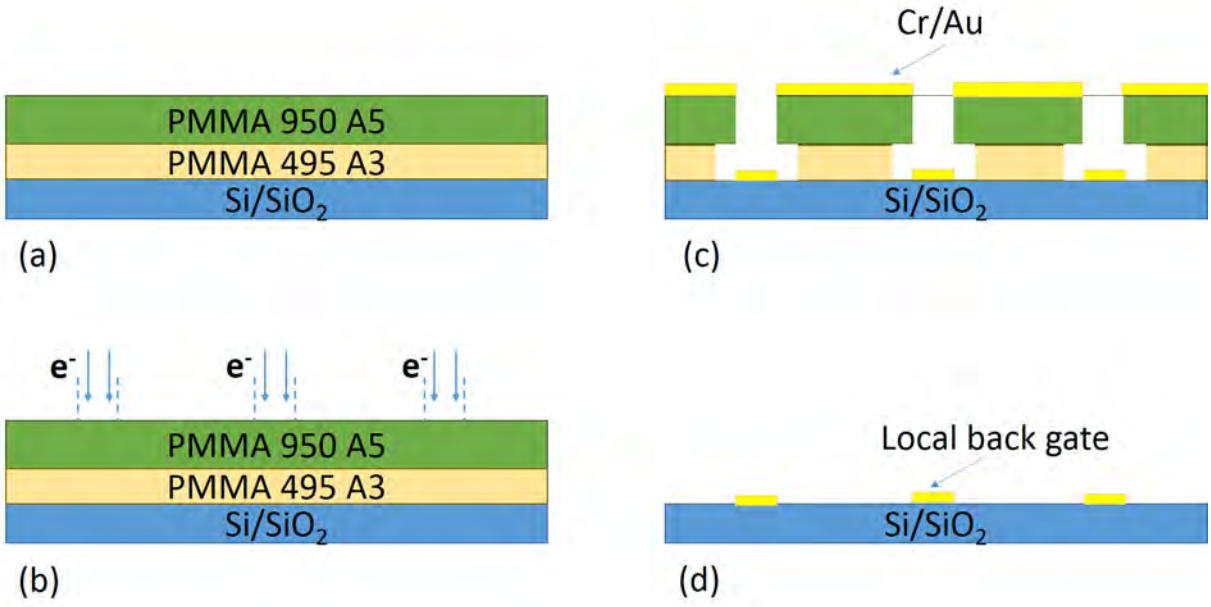


Figure 5: Fabrication procedure of the local back gates. (a) 2 layers of PMMA 495 A3 are spin-coated at 2000 rpm with 500 rpm/sec acceleration for 60 seconds. The substrate is then baked at 170°C for 5 minutes. A new layer of PMMA 950 A5 is then spin-coated onto the substrate at 4000 rpm with 110 rpm/sec acceleration for 70 seconds. The substrate is baked again at 180°C for 4 minutes. (b) The PMMA layers are exposed to e-beam at 450 μC/cm^2 dose. The e-beam exposed PMMA is developed in MIBK:IPA 1:3 solution for 25 seconds and rinsed in IPA for 25 seconds before blown dry in N_2. (c) 5 nm of Cr and 50 nm of Au are deposited on top of the substrate by thermal evaporation. (d) The lift-off process is done by immersing the substrate in cold acetone ($T = 25$°C) for 45 minutes.

D. Process with lift-off resist (LOR)

1. Advantages of using LOR as a dielectric

The design of the locally gated bilayer graphene device requires the graphene to be sandwiched between 2 layers of insulating material. The most readily available materials and deposition methods are summarised in Table II.

LOR (MicroChem) is a polydimethylglutarimide (PMGI) based organic lift-off resist (LOR) that shows stability in the 150°C - 200°C temperature range [14]. Using LOR for the dielectric in the device presents two major advantages. Firstly, the deposition method for LOR is simple. Spin-coating LOR onto the substrate ensures a more uniform dielectric layer while at the same

Material	Deposition method	Dielectric
Thermally grown SiO_2	Thermal evaporation	SiO_2
Aluminium metal	Thermal evaporation	Al_xO_y from oxidisation of aluminium
Hydrogen silsesqioxane (HSQ)	Spin-coating and e-beam exposure	SiO_2-like substance
LOR	Spin-coating	LOR

Table II: A comparison between different materials and deposition methods for the dielectric layers in the bilayer graphene device

time allowing for greater control over its thickness as compared to evaporating silicon dioxide or aluminium metal onto the substrate. Secondly, since the dielectric is the unexposed LOR itself, we can perform an easy post-deposition patterning process for the dielectric layer using photolithography. The photolithography process for LOR involves exposing it to laser beam and developing in MF-319 solution (diluted with DI water in a 1:1 ratio) for 30 seconds (Figure 7b). This process is considerably simpler and involves less harmful chemicals compared to etching oxides of silicon and metals using buffered hydrofluoric acid (BHF), which makes LOR ideal for building locally gated devices with suspended graphene.

The dielectric layer was prepared by spin-coating LOR photoresist onto a Si/SiO_2 wafer at 6000 rpm with angular acceleration 500 rpm/s for 70 seconds. This yields a final thickness of about 300 nm. The LOR-coated wafer was then baked at 170°C for 5 minutes. The patterning of the LOR layer was done by using laser beam at 405 nm wavelength with 100% intensity twice (Figure 8). The pattern was written twice because the beam scan writing mode of the laser writer leaves small unexposed gaps on the photoresist (Figure 9a).

It was found in experiments that LOR is compatible with the developer for PMMA (MIBK solution diluted in IPA in a 1:3 ratio) in the sense that it is not removed together with the PMMA (Figure 7a). This allows us to build the local top gates on top of the LOR layer by e-beam lithography (Figure 6).

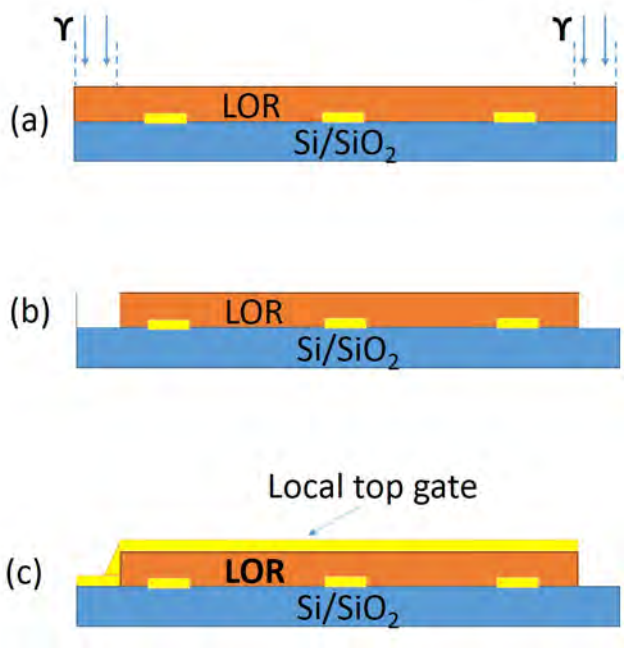


Figure 6: Fabrication procedure of the local top gates with LOR. (a) LOR is spin-coated on top of the local back gates at 6000 rpm with 500 rpm.sec acceleration for 80 seconds. The substrate with LOR is then baked at 170°C for 5 minutes. (b) LOR is exposed to laser beam. The laser exposed LOR is developed in MF-319:DI Water 1:1 solution for 30 seconds and rinsed in DI Water for 30 seconds before blown dry in N_2. (c) The fabrication of the local top gates follows the same steps in Figure 5.

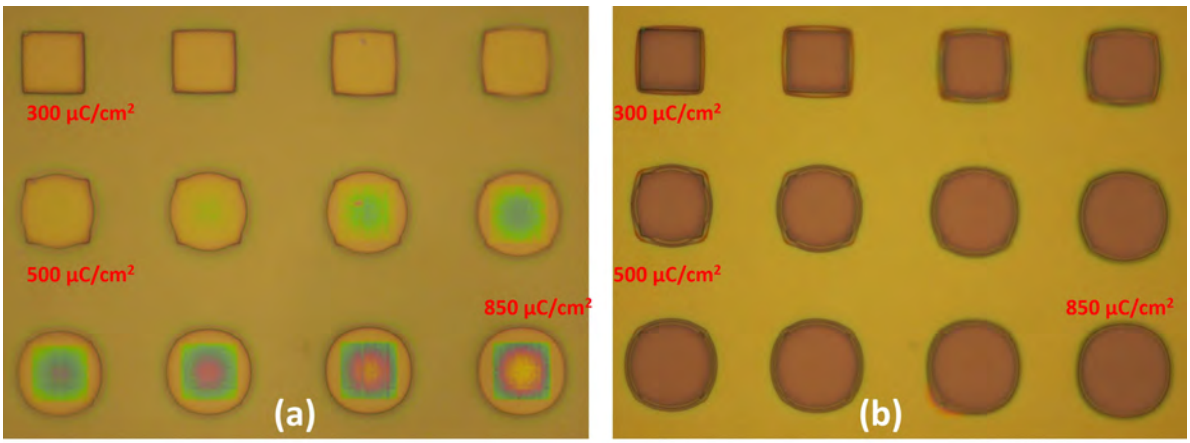


Figure 7: PMMA and LOR exposed to e-beam at various doses. (a) Only e-beam exposed PMMA is developed in MIBK solution. (b) E-beam exposed LOR is developed in MF-319 solution.

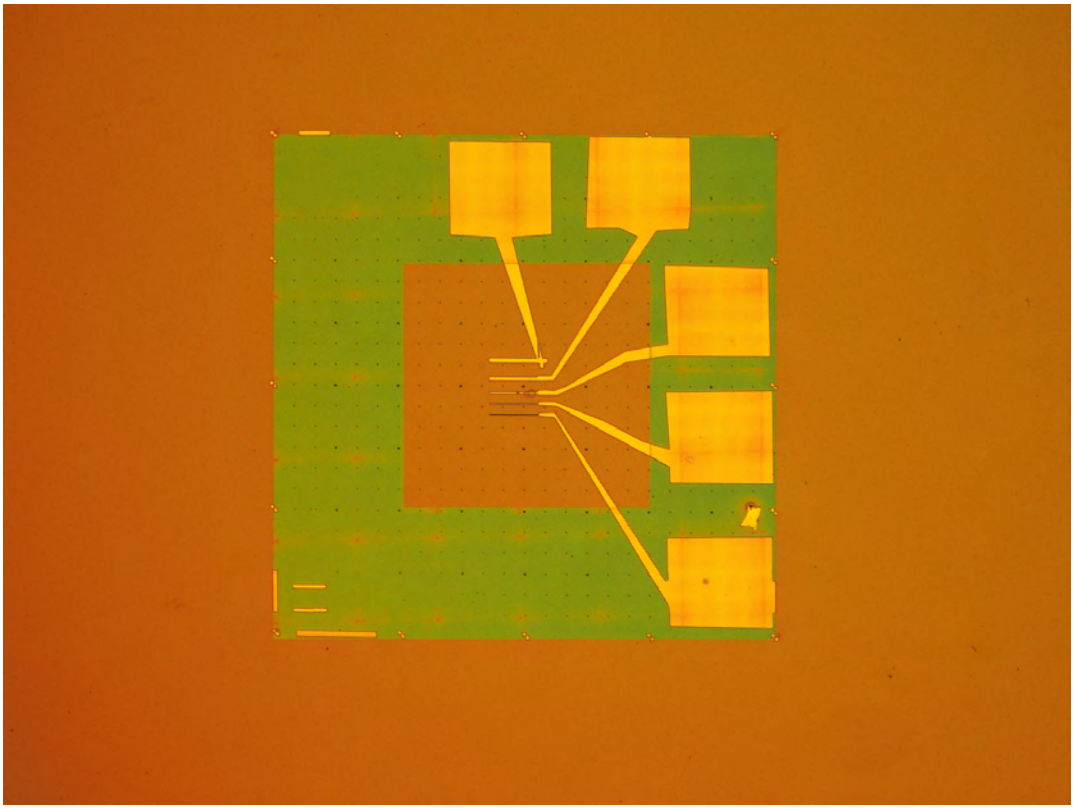


Figure 8: LOR is exposed to 405 nm laser beam at 100% intensity twice in order to make thin the layer of LOR on top of the bonding pads of the local back gates

2. Issues with LOR during fabrication of top gates

It was found in experiments that LOR displays very low absorption of the laser beam at 405 nm wavelength. Figure 9 shows the same pattern written on LOR at 100% and 30% laser intensity (both having the gain value at 35). As can be seen, the contrast is stark. The low absorption of laser beam is not so much a problem as the problem of using the laser at 100% intensity. The pattern written at 30% intensity appears homogeneous (Figure 9b) whereas the pattern written at 100% intensity displays certain degrees of unevenness with narrow, unexposed gaps about 1 μm wide (Figure 9a).

We also ran into a serious problem with the use of acetone during the lift-off process for the top gates. As seen in Figure 11, acetone partially dissolves the areas of LOR that have been exposed to the e-beam.

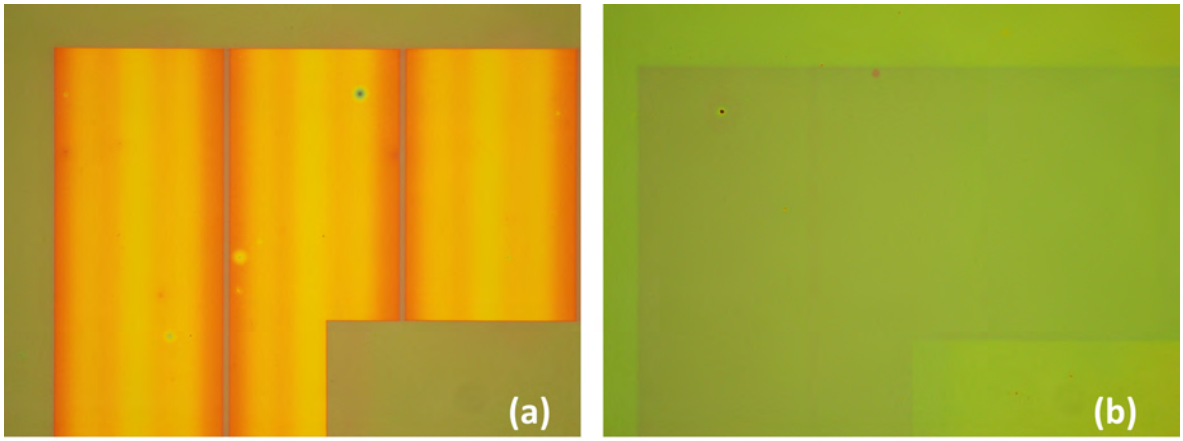


Figure 9: (a) Optical microscope image of the pattern written on LOR with laser beam at 405 nm wavelength and 100% intensity. The surface of the pattern looks uneven with unexposed gaps about 1 μm wide, which may be an indication of inhomogeneity in the laser profile during the writing process. (b) Optical microscope image of the pattern written on LOR with laser beam at 405 nm wavelength and 30% intensity. The pattern displays a more homogeneous profile compared to the patter written at 100% intensity, but also appears underexposed.

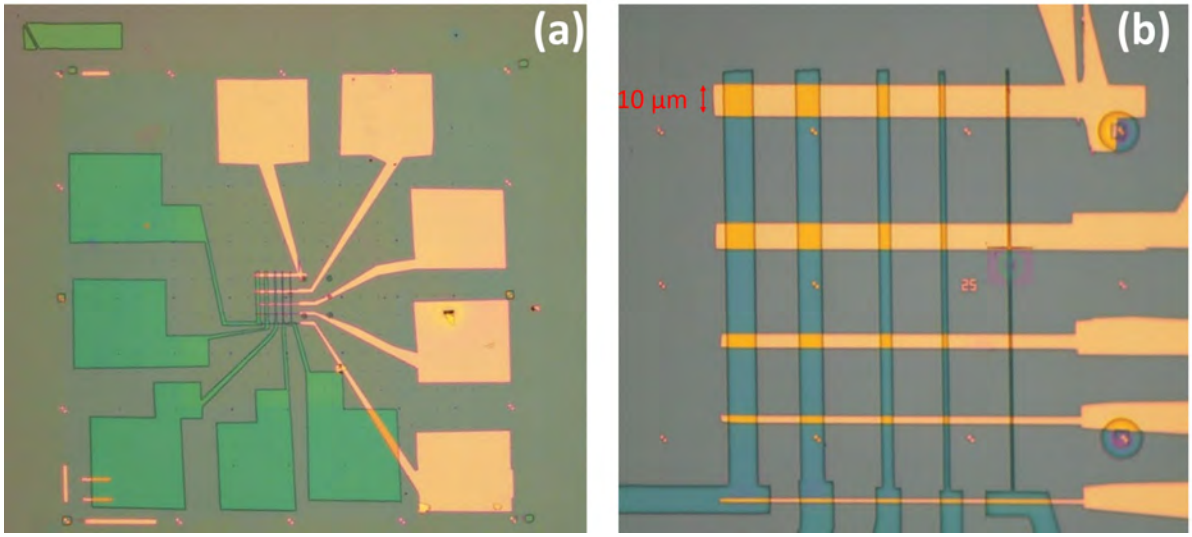


Figure 10: Optical microscope image of a the top gate patterns before metalisation. (a) 5$\times$ magnification: the overlap between the bonding pad for one of the top gates and that of the back gate was a mistake in the design itself; the patterns are properly aligned otherwise. (b) Test device at 50$\times$ magnification

As reported by Tombros *et. al.*, the lift-off process of PMMA on top of LOR can be done by

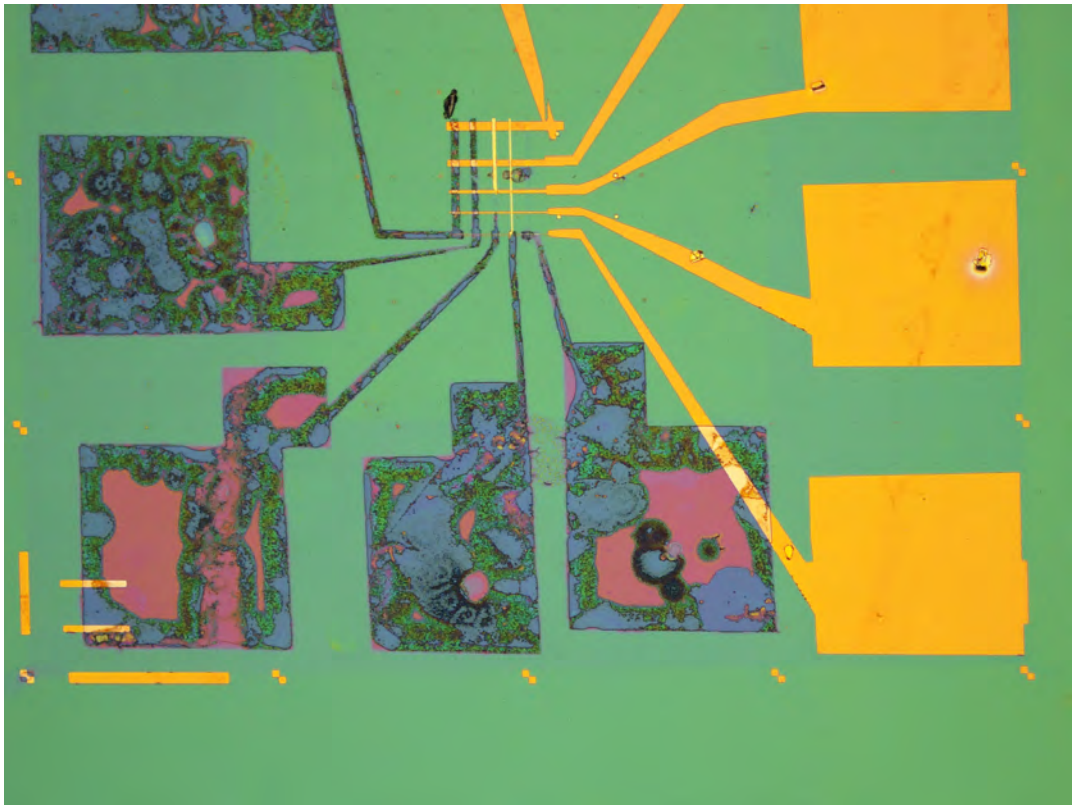


Figure 11: The local top gate patterns ruined by hot acetone ($T = 60°\text{C}$). The hot acetone appears to partially dissolve the e-beam exposed LOR while leaving the unexposed and the laser exposed LOR in tact.

using hot xylene ($T = 80°\text{C}$) [14]. Interestingly, also as reported, xylene at room temperature ($T = 21°\text{C}$) can also be used as a developer for e-beam exposed PMMA [14]. However, xylene was not available to us so new methods had to be devised to circumvent the problem (refer to section 4).

E. Process with hydrogen silsesqioxane (HSQ)

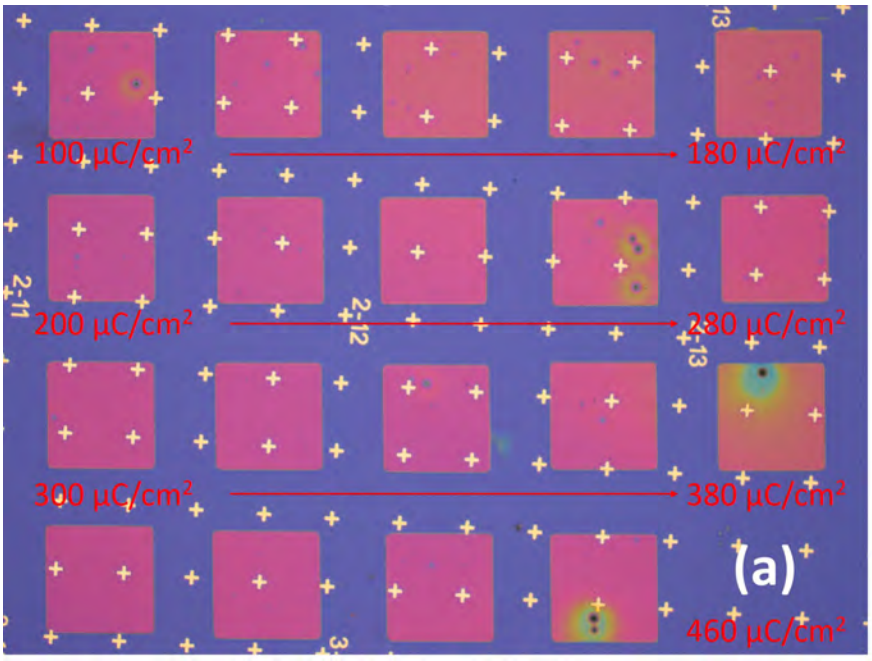
1. E-beam lithography of HSQ

Hydrogen silsesqioxane (HSQ) is a negative e-beam resist that turns into a SiO_2-like substance upon exposure. HSQ has a formula $(HSiO_{3/2})_n$ [15–17]. Isolated polymers of HSQ on thin films will cross-link upon being exposed under e-beam to result in an increase in $Si-O$ to $Si-H$ bonds, which leads to the formation of residue resembling SiO_2 in molecular composition and structure [15, 17]. The exact mechanisms of the cross-linking during e-beam exposure are not well-understood and have been subject of many studies [15, 17].

Here we follow the recipe reported by Georgia Institute of Technology [18]. HSQ was spin-coated onto Si/SiO_2 wafer at 2500 rpm with angular acceleration 500 rpm/sec for 70 seconds. The HSQ-coated wafer was then baked at 250°C for 2 minutes. In order to find the optimal e-beam dose, the HSQ layer was exposed to e-beam at doses from 100 $\mu C/cm^2$ to 1900 $\mu C/cm^2$ (Figure 12).

As seen in figure 12 an e-beam dose of 100 $\mu C/cm^2$ was enough to expose HSQ. The final thickness of the silicon dioxide residue as measured by the atomic force microscope (AFM) is independent of the e-beam dose used, and is typically between 100 nm and 150 nm in agreement to the report by Georgia Institute of Technology [18]. The slight rounding of the corners for the higher doses (1000 $\mu C/cm^2$ to 1900 $\mu C/cm^2$) indicates over-exposure.

It is still unknown how the different e-beam doses may affect the resistivity of the silicon dioxide residue. Hence, for the test structures built, of which there are eight, we will test the resistivity of the silicon dioxide residue for e-beam doses 100, 200, 300, 400, 500, and 1000 $\mu C/cm^2$.



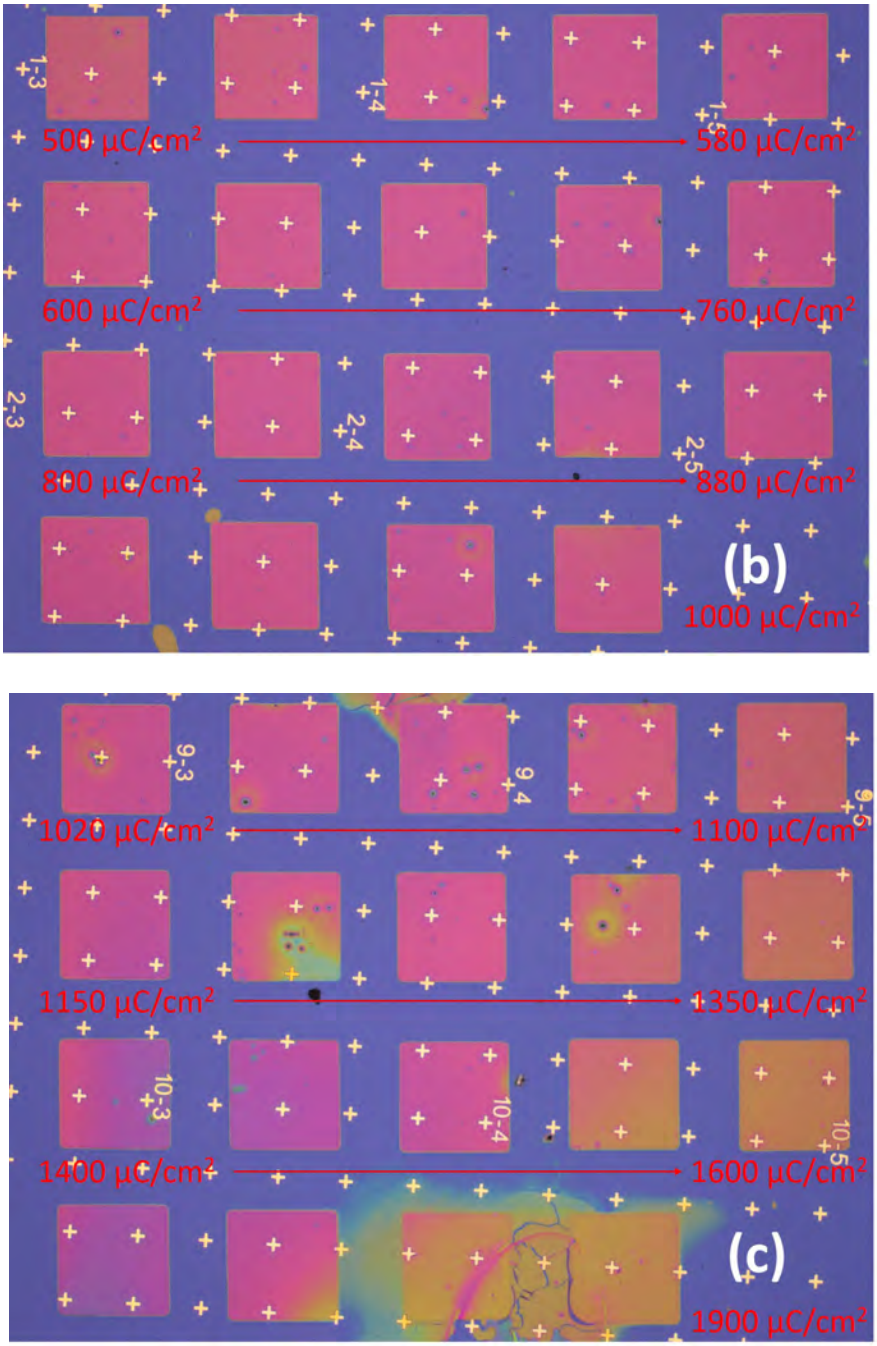


Figure 12: E-beam dose test for HSQ. HSQ was spin-coated onto Si/SiO_2 substrate at 2000 rpm with 500 rpm/sec acceleration for 70 seconds. The e-beam exposures were performed at various doses: (a) 100 - 480 $\mu C/cm^2$, (b) 500 - 1000 $\mu C/cm^2$, and (c) 1020 - 1900 $\mu C/cm^2$.

2. Fabrication of top gates using e-beam lithography

The fabrication of the local top gates on top of the e-beam exposed HSQ layer using e-beam lithography follows the same process as the fabrication of the local back gates using double layers of PMMA (Figure 5). Unlike the fabrication of the back gates, however, here we need to make sure the patterns are properly aligned such that the local top gates only overlap the local back gates in the areas where we want them to. A two-stage alignment process was followed. First, we aligned the patterns using the big markers (5 μm in size) at the four corners of the 1200 $\times$ 1200 μm^2 back gate pattern. Next we used the small markers (1 μm in size) to accurately aligned the patterns. A completed locally gated test structure is shown in Figure 14.

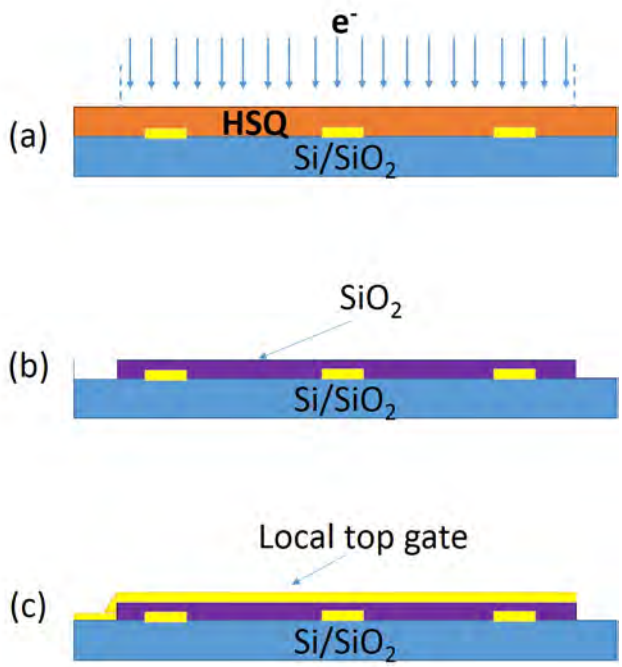


Figure 13: Fabrication procedure of the local top gates with e-beam exposed HSQ. (a) HSQ is spin-coated on top of the local back gates at 2500 rmp to yield a thickness of 100 - 150 μm. (b) HSQ is exposed to e-beam at various doses from 100 - 1900 μC/cm^2. The exposure to e-beam cross-links HSQ molecules which results in an increase in the ratio of $Si-O$ to $Si-H$ bonds, leading to the deposition of a SiO_2-like substance [15]. HSQ is developed in MF-319 solution for 2 minutes and rinsed in DI Water for 30 seconds before blown dry in N_2. (c) The fabrication of the local top gates follows the same steps in Figure 5.

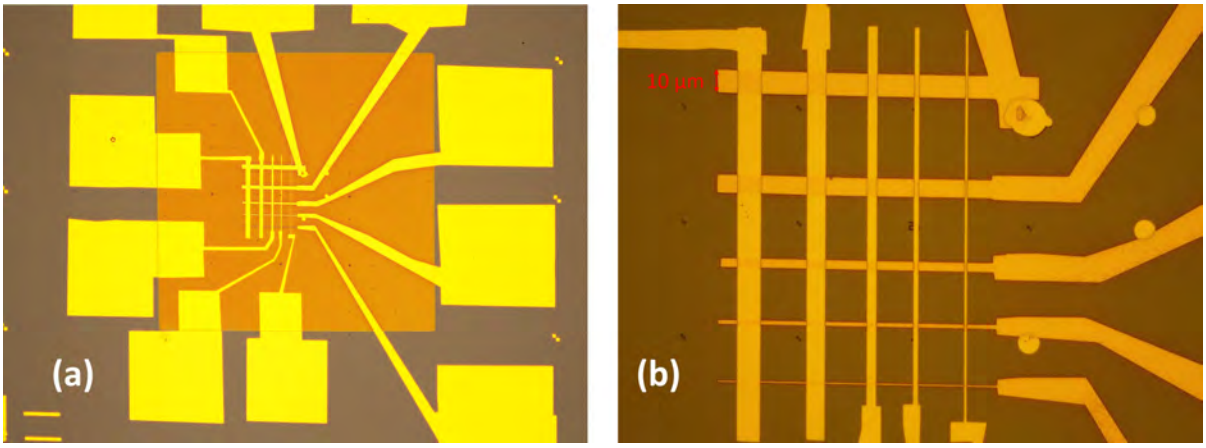


Figure 14: Optical microscope image of a completed locally gated test structure. (a) 10× magnification; photo shows SiO_2-like dielectric layer sandwiched between local back gates and local top gates. (b) 50× magnification; the local top gates and the local back gates in criss-crossing patterns as designed.

IV. CHARACTERISATIONS OF E-BEAM EXPOSED HSQ

A. Layer thickness

HSQ e-beam resist was spin-coated onto the substrate at 2500 rpm at 500 rpm/sec acceleration for 70 seconds. The resist was exposed to e-beam with doses at 100, 200, 300, 400, 500, and 1000 μC/cm^2. The thickness of the e-beam exposed HSQ layer after development in MF319 was measured by using the atomic force microscope. The results are summarised in Table III.

E-beam dose (μC/cm^2)	**Layer thickness (nm)**
100	120 ± 10
200	128 ± 10
300	127 ± 10
400	117 ± 10
500	130 ± 10
1000	123 ± 10

Table III: The thickness of the e-beam exposed HSQ layer

The dose of the e-beam under which HSQ was exposed seems to have little control over the

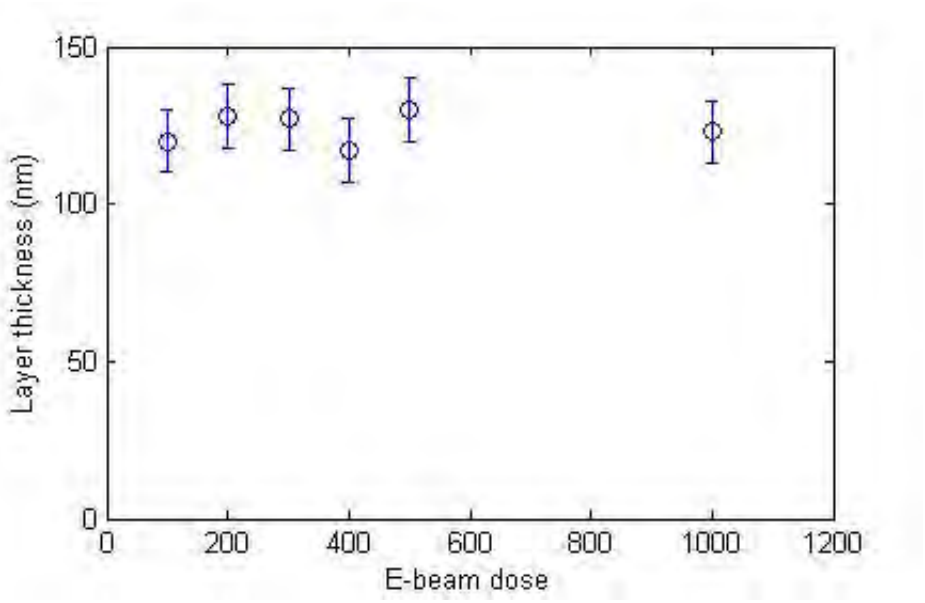


Figure 15: A graph showing the thickness of the e-beam exposed HSQ layer against the e-beam dose. The scatter plot shows no apparent relationship between the layer thickness and the e-beam dose.

thickness of the e-beam exposed HSQ deposits (Figure 15). A lower e-beam dose will speed up the fabrication process. For now we can conclude that as far as layer thickness is concerned, an e-beam dose as low as 100 μC/cm^2 may be used. To characterise e-beam exposed HSQ as a dielectric to used in a graphene device, however, one still needs to perform electrical measurements and test whether the e-beam doses used during the fabrication process have any effect on the electrical properties of the e-beam exposed HSQ.

B. Breakdown voltage

The breakdown voltage was measured at room temperature ($T \approx 25^\circ$C) for HSQ resist that was exposed to e-beam at 1000 μC/cm^2 dose. Here we define the voltage at which the current exceeds 100 nA as the breakdown voltage. The local top gates were subject to a positive voltage with increasing values from 0.0 V to 20.0 V. The local back gates were grounded in all experiments. A typical I-V characteristic curve of most intersections on the test device is shown in Figure 16. Sharp spikes are sometimes observed in an I-V characteristic curve (Figure 17). The sharp spikes indicate small, short-lived leakage currents, but how they form and terminate remains largely a question. The measurements of the breakdown voltage are summarised in Table IV.

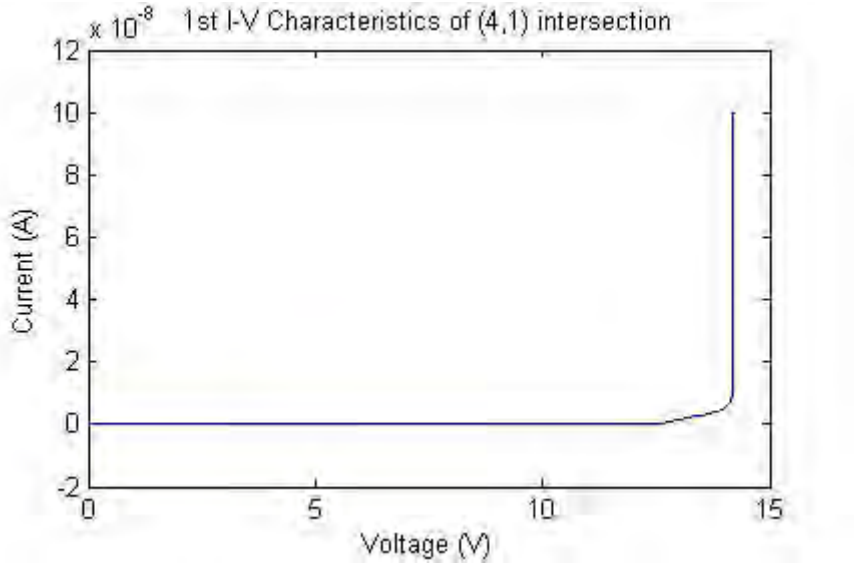


Figure 16: I-V characteristic curve of for the (4,1) intersection of the test device (refer to Figure 3). We define a current larger than 100 nA as the leakage current and the corresponding voltage as the breakdown voltage. The breakdown voltage is 14.1 V for the (4,1) intersection.

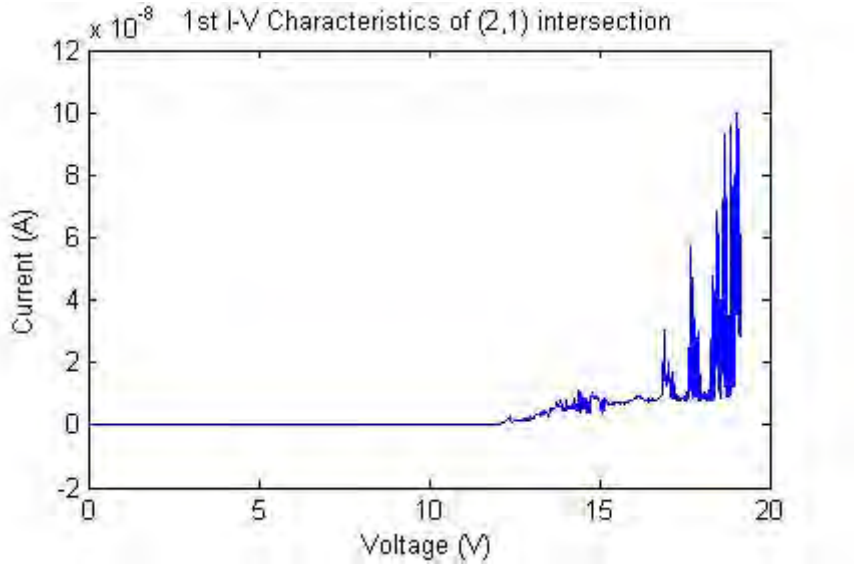


Figure 17: I-V characteristic curve of for the (2,1) intersection of the test device (refer to Figure 3). The breakdown voltage is 17.7 V for the (2,1) intersection; however, small and short-lived leakage currents have developed at lower voltages as can be seen from the sharp spikes in the I-V characteristic curve.

Position	**Cross-section area** (μm^2)	**Breakdown voltage** V (V)	**Bulk resistivity** ρ ($\times 10^{16}\Omega$*nm)
$(1,1)$	10×10	16.2	1.75 ± 0.17
$(1,2)$	10×8	> 20.0	1.99 ± 0.18
$(1,3)$	10×4	> 20.0	0.76 ± 0.12
$(1,4)$	10×2	> 20.0	0.63 ± 0.08
$(1,5)$	10×1	18.7	0.47 ± 0.05
$(2,1)$	8×10	17.7	2.84 ± 0.33
$(2,2)$	8×8	18.7	2.80 ± 0.36
$(2,3)$	8×4	> 20.0	0.71 ± 0.69
$(2,4)$	8×2	> 20.0	0.82 ± 0.24
$(2,5)$	8×1	19.2	0.14 ± 0.01
$(3,1)$	4×10	13.6	1.43 ± 0.17
$(3,2)$	4×8	13.8	0.67 ± 0.08
$(3,3)$	4×4	12.9	0.63 ± 0.06
$(3,4)$	4×2	17.7	0.35 ± 0.05
$(3,5)$	4×1	13.7	0.11 ± 0.01
$(4,1)$	2×10	14.1	0.50 ± 0.08
$(4,2)$	2×8	11.6	0.57 ± 0.06
$(4,3)$	2×4	14.5	0.36 ± 0.04
$(4,4)$	2×2	17.0	0.12 ± 0.01
$(4,5)$	2×1	17.9	0.06 ± 0.005
$(5,1)$	1×10	> 20.0	0.27 ± 0.04
$(5,2)$	1×8	18.1	0.34 ± 0.03
$(5,3)$	1×4	8.5	0.13 ± 0.02
$(5,4)$	1×2	12.5	0.06 ± 0.005
$(5,5)$	1×1	7.8	0.03 ± 0.003

Table IV: The breakdown voltage and the bulk resistivity of different intersections on the test device

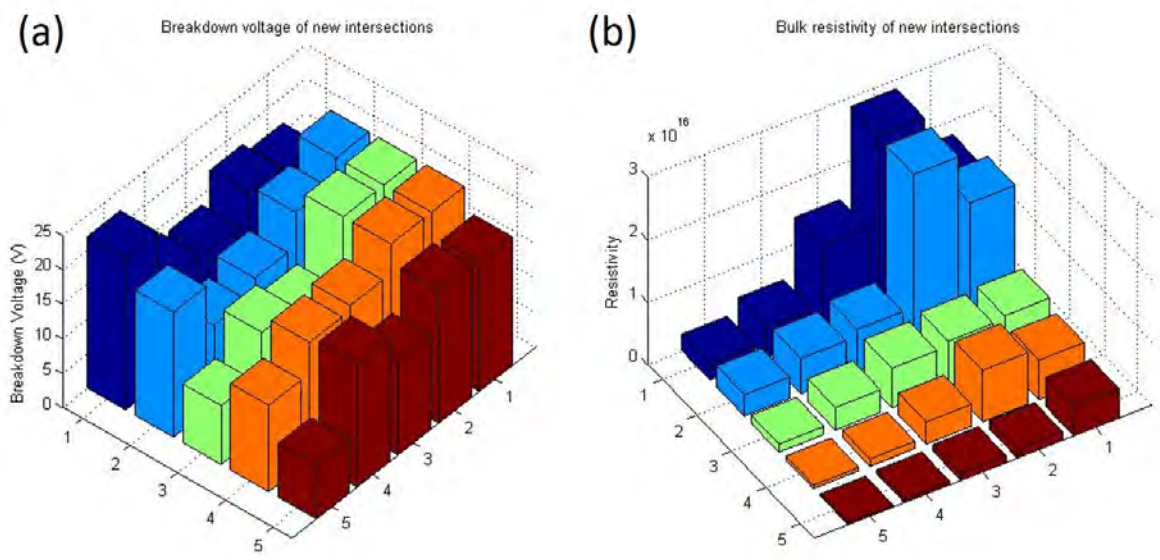


Figure 18: (a) The breakdown voltage at different intersections on the test device. The breakdown voltage is higher for larger intersections. (b) The bulk resistivity (measured in Ω*nm) of different intersections follows a similar trend as the breakdown voltage: higher at larger intersections and dipping towards the smallest intersection.

The diagrams in Figure 18 display the breakdown voltage and the bulk resistivity of different intersections on the test device. A value of 22.0 V was assigned to the breakdown voltages that are larger than 20.0 V. A similar general trend can spotted for both diagrams, that is, the values of the breakdown voltage and the bulk resistivity are higher for larger intersections and the data dip towards the smallest intersection of 1 μm^2 at $(5, 5)$.

C. Resistivity measurements

1. New devices

The resistance of each intersection of e-beam exposed HSQ is calculated from the I-V data. The data is normalised by taking out the off-set current. The mean resistance is calculated by averaging resistance data between 0.5 V and 1.0 V, which is a part of the Ohmic section in all I-V characteristic curves obtained. The Ohmic section of a new intersection can extend up to 12.0 V, whereas that of a damaged intersection (a device that has been subject to breakdown voltage) is typically limited to low voltages between 0.0 V and 2.0 V (Figure 19).

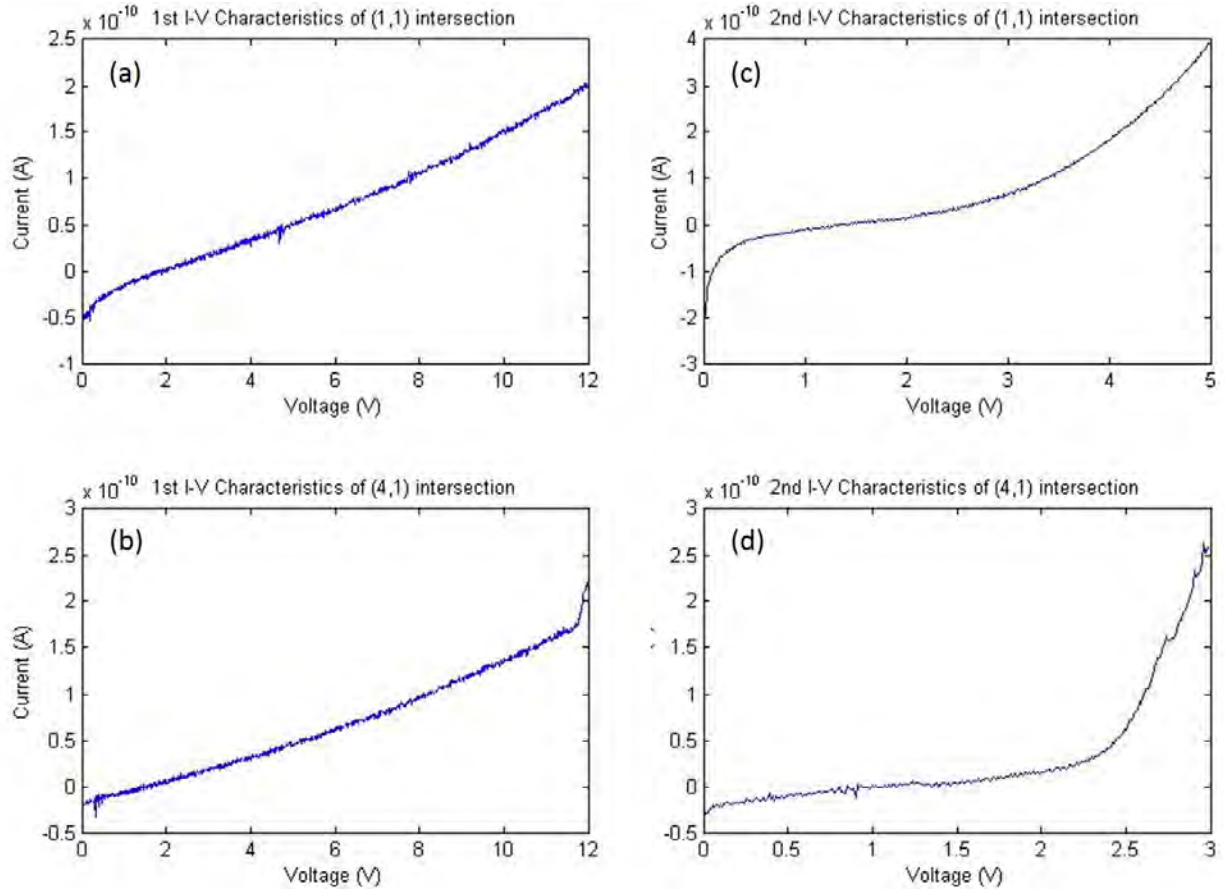


Figure 19: (a) and (b) $I-V$ characteristic curves of new (1,1) and (4,1) intersections. The graph displays an almost linear behaviour until the voltage reaches about 12.0 V. (c) and (d) $I-V$ characteristic curves of damaged (1,1) and (4,1) intersections. The graph shows highly non-linear behaviours. The Ohmic section, in contrast to that of new intersections, is limited to low voltages up to 2.0 V.

2. Damaged intersections

It is also of interest to us to characterise the electrical resistivity of the e-beam exposed HSQ after a catastrophic event, such as a leakage current, has occurred. As leakage current typically caused some degrees of structural damage to the local top gates (Figure 20). In addition, as can be seen in Figure 20, the high voltage applied to the top gates also caused the e-beam exposed HSQ dielectric to lose some of its structural and/or compositional integrity. Such damage to the top gates and the dielectric layer may have an impact on the electrical resistivity of the intersection. Table V compares experimental values of the bulk resistivity of new and damaged intersections.

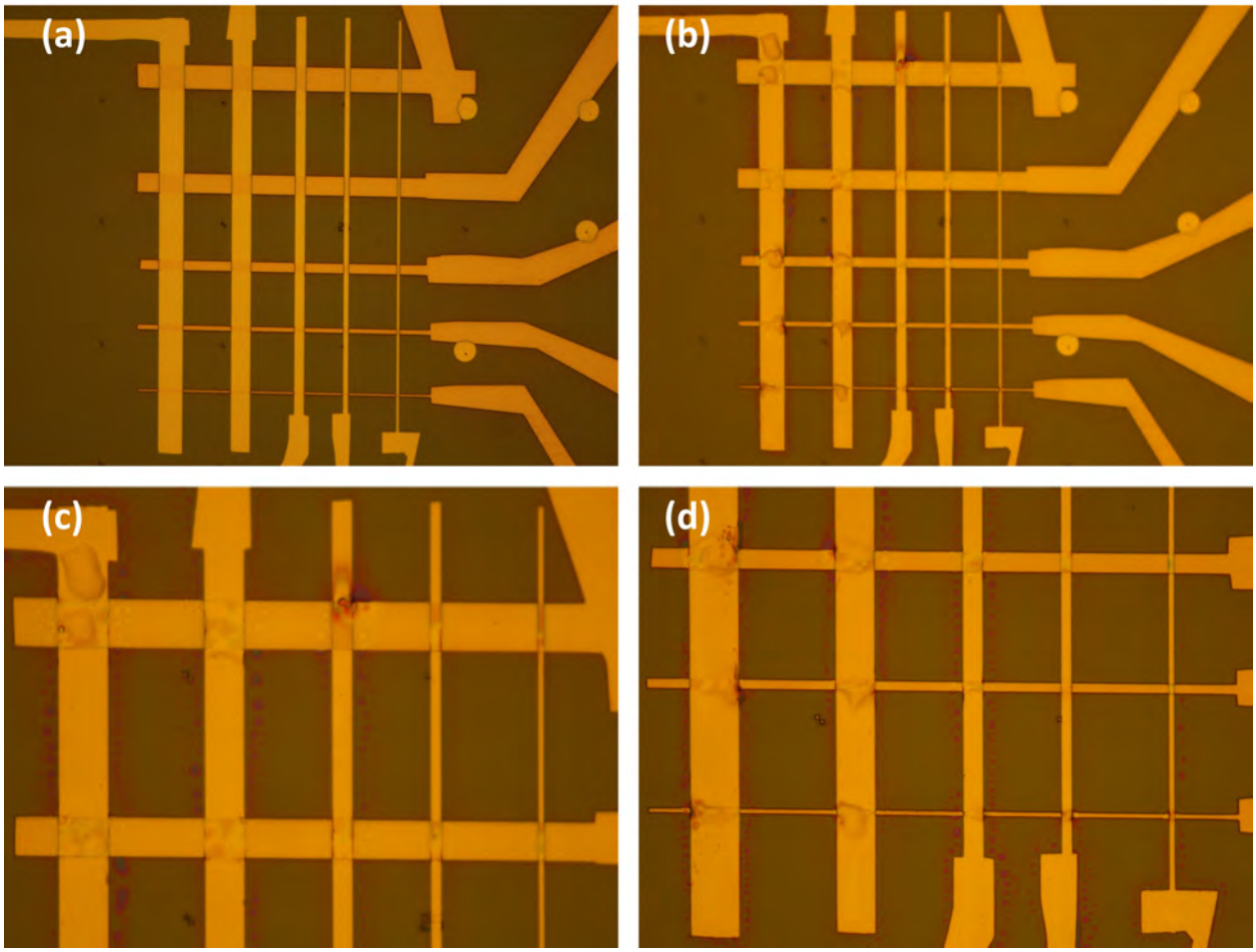


Figure 20: (a) $50\times$ optical microscope image of the test device before experiencing leakage currents at high voltages. (b) $50\times$ optical microscope image of the damaged test device after experiencing leakage currents. (c) and (d) $100\times$ optical microscope images of the test device. The images show bubble-like topography on the top gate at the intersections. The e-beam exposed HSQ dielectric also displays colour changes that may have resulted from structural and/or compositional damages for being subject to high voltages.

The diagrams in Figure 21 compare the bulk resistivity measured for new and damaged intersections. The bulk resistivity values of the damaged intersections are lower across the board than those of the new intersections, with an exception of the $(1, 3)$ intersection where the bulk resistivity increases for the damaged intersection.

Intersection	**Cross-section area** (μm^2)	**Bulk resistivity of new intersection** ρ_0 ($\times 10^{16}\Omega$*nm)	**Bulk resistivity of damaged intersection** ρ_d ($\times 10^{16}\Omega$*nm)
$(1,1)$	10×10	1.75 ± 0.17	0.23 ± 0.04
$(1,2)$	10×8	1.99 ± 0.18	0.33 ± 0.06
$(1,3)$	10×4	0.76 ± 0.12	1.04 ± 0.07
$(1,4)$	10×2	0.63 ± 0.08	0.38 ± 0.03
$(1,5)$	10×1	0.47 ± 0.05	0.03 ± 0.005
$(2,1)$	8×10	2.84 ± 0.33	0.28 ± 0.05
$(2,2)$	8×8	2.80 ± 0.36	0.12 ± 0.02
$(2,3)$	8×4	0.71 ± 0.69	0.16 ± 0.03
$(2,4)$	8×2	0.82 ± 0.24	0.51 ± 0.05
$(2,5)$	8×1	0.14 ± 0.01	0.03 ± 0.004
$(3,1)$	4×10	1.43 ± 0.17	0.17 ± 0.03
$(3,2)$	4×8	0.67 ± 0.08	0.16 ± 0.03
$(3,3)$	4×4	0.63 ± 0.06	0.06 ± 0.01
$(3,4)$	4×2	0.35 ± 0.05	0.04 ± 0.007
$(3,5)$	4×1	0.11 ± 0.01	0.02 ± 0.004
$(4,1)$	2×10	0.50 ± 0.08	0.0007 ± 0.0001
$(4,2)$	2×8	0.57 ± 0.06	0.07 ± 0.01
$(4,3)$	2×4	0.36 ± 0.04	0.04 ± 0.007
$(4,4)$	2×2	0.12 ± 0.01	0.02 ± 0.004
$(4,5)$	2×1	0.06 ± 0.005	0.04 ± 0.006
$(5,1)$	1×10	0.27 ± 0.04	0.29 ± 0.04
$(5,2)$	1×8	0.34 ± 0.03	0.04 ± 0.007
$(5,3)$	1×4	0.13 ± 0.02	0.02 ± 0.003
$(5,4)$	1×2	0.06 ± 0.005	0.004 ± 0.0007
$(5,5)$	1×1	0.03 ± 0.003	0.005 ± 0.0009

Table V: The thickness of the e-beam exposed HSQ layer

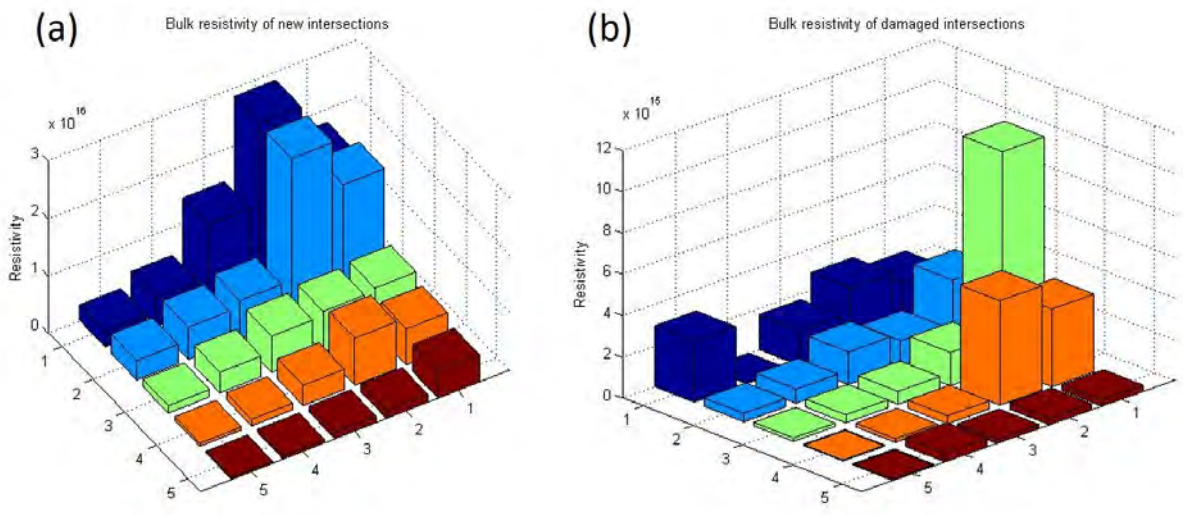


Figure 21: (a) The bulk resistivity (measured in Ω*nm) of new intersections. (b) The bulk resistivity (measured in Ω*nm) of damaged intersections.

The experimental data strongly suggest that electrical damages due to leakage currents would likely cause a reduction in the bulk resistivity of an intersection. Nevertheless, there is another type of electrical damage in the experiments which is the damage caused when the dielectric was subject to the high voltages of the top gates over an extended amount of time. The former type of damage only lasts for a short duration and is likely the one responsible for the formation of the bubble-like topography on the top gates, whereas the latter is more likely responsible for the colour changes observed in regions of the dielectric around the edges of the top gates. While the data is quite conclusive that the leakage currents caused the observed reduction in the resistivity, we do not have sufficient data to conclude whether the slow electrical damage to the dielectric when subject to high voltages would have the same effect on the bulk resistivity of the dielectric.

Due to the geometry laid out by the electrical contacts in the test device (refer to Figure 20a), electrical measurements were performed on the $(5, 1)$ intersection first and on the $(5, 5)$ intersection last. Thus, by the time measurements were taken, the $(5, 5)$ intersection had been subject to high voltages from the top gates for a significant amount of time and we can expect that the dielectric at the $(5, 5)$ intersection, to a certain extent, had been compromised structurally and/or compositionally. The low breakdown voltages and bulk resistivity both for new and damaged intersections observed for the smaller intersections could be the overall effects of both

types of electrical damage on the resistivity, and they seem to suggest that both types of electrical damage have the same reducing effect on the bulk resistivity.

Based on the breakdown voltage data that we have, and taking into account the observation that small, short-lived leakage currents can form before the breakdown voltage, we can propose that the maximum working voltage that is safe for the e-beam exposed HSQ deposits would be 5.0 V. More tests are needed still to determine how long the e-beam exposed HSQ dielectric can withstand a voltage across it before breaking down.

V. UNRESOLVED ISSUES AND FUTURE WORKS

A. Effects of contact time on resistivity of e-beam exposed HSQ deposits

The contact time here refers to the time the e-beam exposed HSQ deposits lies in contact with an electrode which is maintained at a voltage. Our electrical characterisations of the e-beam exposed HSQ dielectric have established a working voltage range at room temperature that is safe for the deposits. As mentioned in the previous section, we must also find a working time frame for the dielectric. As discussed before, long contact time with high voltages will degrade the e-beam exposed HSQ slowly. This may cause a decrease in the resistivity of the substance as observed and, thus, increase the chance of leakage current flowing through the dielectric layer.

B. Effects of e-beam doses on resistivity of HSQ deposits

The resistivity data were collected for the HSQ deposits exposed to e-beam at 1000 μC/cm^2 dose. In order to maximise the fabrication process involving HSQ, more experiments are needed to test the effects of different e-beam doses on the resistivity of the completed device.

C. Measuring electrical resistivity of LOR

Given the advantages of using LOR, it is worthwhile to study its resistivity in order to implement it in a locally gated graphene device. One possible way to circumvent the problem we faced with acetone affecting e-beam exposed LOR is to use laser lithography process to pattern the top gates with SU8 2000.5 - a negative photoresist that can be lifted off in acetone. The fabrication

procedure for the process involving SU8 2000.5 (outlined in Figure 22) does not involve exposing LOR to e-beam. Hence, this method may help avoid the problem with acetone (acetone does not affect unexposed and laser exposed LOR).

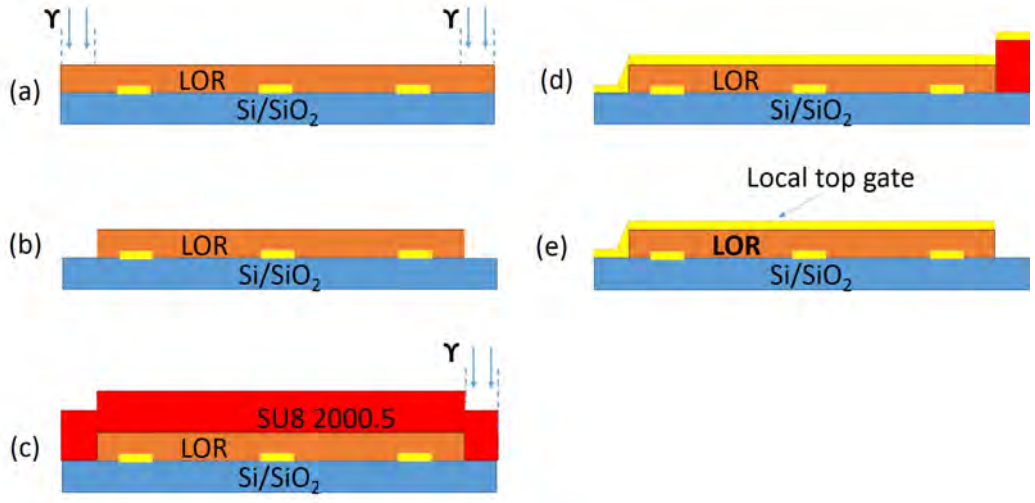


Figure 22: Fabrication procedure of the local top gates with SU8 2000.5. (a) LOR is exposed to laser beam using lens 4 with gain 35 and no filter. (b) The laser exposed LOR is developed in MF-319:DI Water 1:1 solution for 30 seconds and rinsed in DI Water for 30 seconds before blown dry in N_2. (c) SU8 2000.5 is spin-coated on top of LOR at 3000 rpm with 500 rpm/sec acceleration for 70 seconds to yield a thickness of 500 nm. SU8 2000.5 is developed using the SU8 developer. The exposed areas will be developed leaving the exposed regions behind. (d) The device is subject to metalisation step; 5 nm of Cr and 50 nm of Au are deposited thermally onto the LOR and SU8 2000.5 layers. (e) Exposed SU8 2000.5 is lifted off in acetone.

However, there still remain 2 problems that need to be addressed before we can confirm the feasibility of this fabrication procedure. Firstly, we need to establish firmly that after metalisation, SU8 2000.5 can indeed be lifted off in acetone. Secondly, SU8 2000.5 also displays low absorption of laser beam at 405 nm wavelength to the extent that exposures at 100% intensity had to be done 8 times to write a pattern. This demands that the problem of writing with the laser beam at full intensity be fixed.

There may be an easy way to bypass the writing problem by writing the same pattern once in the vertical direction and once in the horizontal direction so as to minimise the unexposed area (Figure 8). However, while it is easy with the LOR layer given the symmetry of the pattern, the

task will be more involved with the design of the top gates, and even if such a task can be done, we still have the risk of unexposed areas making unwanted connections in the circuit.

D. Locally gated graphene device

The ultimate goal is build a locally gated graphene device with suspended bilayer graphene (Figure 2). Since we know the composition and structure of e-beam exposed HSQ approximate SiO_2, a standard wet etching in buffered hydrofluoric acid (BHF) precedure can, thus, be followed to construct a suspended device. A PMMA mask lets HF come into contact with the HSQ deposits following a designed pattern, allowing us to control where the etching will occur. Figure 23 shows a proposed fabrication procedure to build a suspended device by wet etching e-beam exposed HSQ in BHF. Testing is needed to determine the rate at which BHF undercuts the e-beam exposed HSQ and, hence, the amount of time needed for etching.

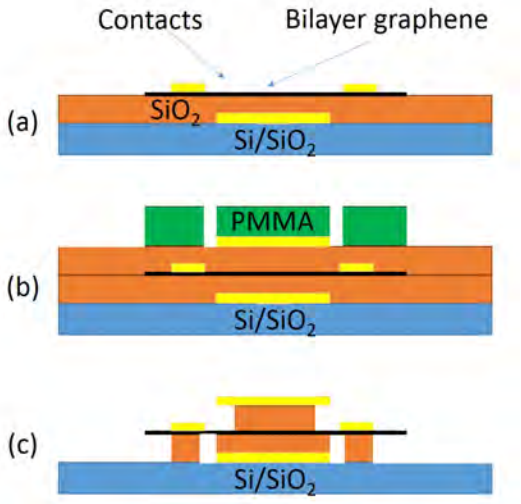


Figure 23: Proposed fabrication procedure for building suspended devices by wet etching e-beam exposed HSQ in BHF. (a) Bilayer graphene sheet is deposited on top of the first e-beam exposed HSQ layer. The electrical contacts are built by following the steps outlined in Figure 5. (b) A PMMA mask is put on top of the second e-beam exposed HSQ layer and the local top gate. BHF will come into contact with the regions of e-beam exposed HSQ that are not covered by the PMMA mask. (c) Suspended device after wet etching in BHF.

VI. CONCLUSIONS

In this report, we presented two fabrication processes for a locally gated test device: one using LOR, a photoresist that can be patterned by both laser and e-beam lithography techniques, and the other using HSQ, a negative e-beam resist that leaves a durable layer of SiO_2-like layer upon being exposed to e-beam. Both processes have their own advantages and disadvantages. For a process involving LOR, we can avoid the use of hydrofluoric acid for etching when we build a suspended structure. However, xylene and ethyllactate are needed for the development and lift-off steps in the fabrication process [17]. On the other hand, if we choose the process involving HSQ, standard e-beam lithography techniques with lift-off in acetone can be followed as demonstrated by the fabrication of our test devices. The disadvantage of using HSQ is that it requires the use of hydrofluoric acid at a later stage when we proceed to build suspended structures.

The process we developed in this project can be applied to the fabrication of a locally gated device with suspended graphene. For a suspended graphene device, a transfer mechanism similar to the one developed by Grushina *et al.* (2013) [7] will be needed to position a graphene sheet on top of the local back gates. Wet etching in buffered hydrofluoric acid is required to build suspended structures should we choose e-beam exposed HSQ as a dielectric. Otherwise, should we choose LOR as an insulating substance for the graphene device, an e-beam lithography process can be developed.

The characterisation tests we performed on the e-beam exposed HSQ deposits show that the material can withstand high voltages (the lowest is 7.8 V while the highest is more than 20.0 V) at room temperature before reaching the breakdown voltage. The resistance of all intersections on the test device was consistently in order of 10 GΩ. At extreme voltages, there are two types of electrical damages to the e-beam exposed HSQ dielectric that were observed: one is the damage due to the leakage current at the breakdown voltage, and the other is the damage suffered by the dielectric when subject to a high voltage over an extended amount of time. The experimental bulk resistivity data show quite conclusively that an electrical damage caused by a leakage current to the dielectric will reduce the resistivity of the dielectric. It is, however, still unclear whether or not the slow damage due to high voltages would have the same reducing effect on the resistivity.

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APPENDIX A: LOR-3A LASER LITHOGRAPHY RECIPE

The laser lithography recipe for LOR-3A photoresist is summarised in Table VI

Spin-coating speed(s)	6000 rpm with 500 rpm/sec acceleration for 80 sec
Pre-bake temperature	170°C for 5 min
Laser wavelength	405 nm
Laser intensity	100 %
Laser gain	35
Development	MF-319:DI Water 1:1 for 30 sec, then rinsed in DI Water for 30 sec before blown dry
Remarks	Patterns need writing twice

Table VI: Laser lithography recipe for LOR-3A

APPENDIX B: HSQ E-BEAM LITHOGRAPHY RECIPE

The e-beam lithography recipe for HSQ resist is summarised in Table VII

Spin-coating speed(s)	2500 rpm with 500 rpm/sec acceleration for 70 sec
Pre-bake temperature	250°C for 2 min
E-beam voltage	30 kV
E-beam area dose	$100 - 1000$ μC/cm^2
Development	MF-319 for 2 minutes, then rinsed in DI Water for 30 sec before blown dry

Table VII: E-beam lithography recipe for HSQ

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